

FEATURES

- ▶ RF 2 × 2 transceiver with integrated 12-bit DACs and ADCs
- ▶ Frequency band: 70 MHz to 6.0 GHz
- ▶ Supports TDD and FDD operation
- ▶ Tunable channel bandwidth: <200 kHz to 56 MHz
- ▶ Dual receivers: 6 differential inputs or 12 single-ended inputs
- ▶ Superior receiver sensitivity with a noise figure of 2 dB at 800 MHz LO
- ▶ RX gain control
 - ▶ Real-time monitor and control signals for manual gain
 - ▶ Independent automatic gain control
- ▶ Dual transmitters: 4 differential outputs
- ▶ Highly linear broadband transmitter
 - ▶ TX EVM: ≤-40 dB
 - ▶ TX noise: ≤-157 dBm/Hz noise floor
 - ▶ TX monitor: ≥66 dB dynamic range with 1 dB accuracy
- ▶ Integrated fractional-N synthesizers
 - ▶ 2.4 Hz maximum local oscillator (LO) step size
- ▶ Multichip synchronization
- ▶ CMOS/LVDS digital interface

APPLICATIONS

- ▶ Point to point communication systems
- ▶ Femtocell/picocell/microcell base stations
- ▶ General-purpose radio systems

GENERAL DESCRIPTION

The MCT9361 is a high performance, highly integrated radio frequency (RF) Agile Transceiver designed for use in 3G and 4G base station applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The MCT9361 operates in the frequency range of 70 MHz to 6.0 GHz, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

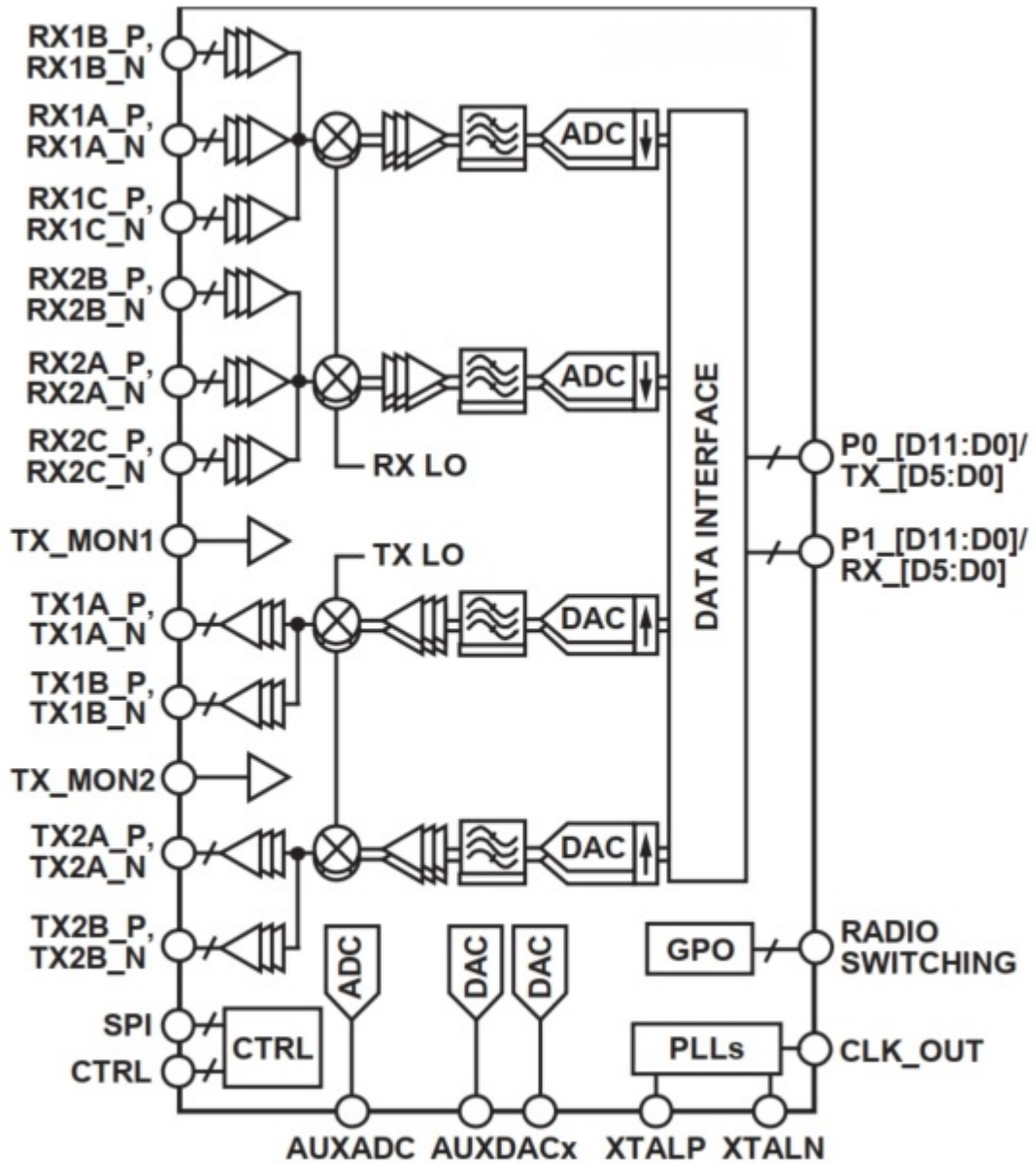
The two independent direct conversion receivers have state-of-the-art noise figure and linearity. Each receive (RX) subsystem includes independent automatic gain control (AGC), dc offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The MCT9361 also has flexible manual gain modes that can be externally controlled. Two high dynamic range analog-to-digital converters (ADCs) per channel digitize the received I and Q signals and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate.

The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a TX error vector magnitude (EVM) of <-40 dB, allowing significant system margin for the external power amplifier (PA) selection. The on-board transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurements.

The fully integrated phase-locked loops (PLLs) provide low power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation, demanded by frequency division duplex (FDD) systems, is integrated into the design. All VCO and loop filter components are integrated.

The core of the MCT9361 can be powered directly from a 1.3 V regulator. The IC is controlled via a standard 4-wire serial port and four real-time input/output control pins. Comprehensive power-down modes are included to minimize power consumption during normal use. The MCT9361 is packaged in a 10 mm × 10 mm, 144-ball BGA package.

FUNCTIONAL BLOCK DIAGRAM



NOTES

1. SPI, CTRL, P0 [D11:D0]/TX [D5:D0], P1 [D11:D0]/RX [D5:D0], AND RADIO SWITCHING CONTAIN MULTIPLE PINS.

Figure 1.

SPECIFICATIONS

Electrical characteristics at VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, and all other VDDx pins = 1.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter ¹	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
RECEIVERS, GENERAL						
Center Frequency		70		6000	MHz	
Gain						
Minimum			0		dB	
Maximum			74.5		dB	At 800 MHz
			73.0		dB	At 2300 MHz (RX1A, RX2A)
			72.0		dB	At 2300 MHz (RX1B, RX1C, RX2B, RX2C)
			65.5		dB	At 5500 MHz (RX1A, RX2A)
Gain Step			1		dB	
Received Signal Strength Indicator	RSSI					
Range			100		dB	
Accuracy			±2		dB	
RECEIVERS, 800 MHz						
Noise Figure	NF		2		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-18		dBm	Maximum RX gain
Second-Order Input Intermodulation Intercept Point	IIP2		40		dBm	Maximum RX gain
Local Oscillator (LO) Leakage			-122		dBm	At RX front-end input
Quadrature						
Gain Error			0.2		%	
Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			-42		dB	19.2 MHz reference clock
Input S ₁₁			-10		dB	
RX1 to RX2 Isolation						
RX1A to RX2A, RX1C to RX2C			70		dB	
RX1B to RX2B			55		dB	
RX2 to RX1 Isolation						
RX2A to RX1A, RX2C to RX1C			70		dB	
RX2B to RX1B			55		dB	
RECEIVERS, 2.4 GHz						
Noise Figure	NF		3		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-14		dBm	Maximum RX gain
Second-Order Input Intermodulation Intercept Point	IIP2		45		dBm	Maximum RX gain
LO Leakage			-110		dBm	At receiver front-end input
Quadrature						
Gain Error			0.2		%	
Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			-42		dB	40 MHz reference clock
Input S ₁₁			-10		dB	
RX1 to RX2 Isolation						
RX1A to RX2A, RX1C to RX2C			65		dB	

SPECIFICATIONS

Table 1. (Continued)

Parameter ¹	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
RX1B to RX2B			50		dB	
RX2 to RX1 Isolation						
RX2A to RX1A, RX2C to RX1C			65		dB	
RX2B to RX1B			50		dB	
Logic Outputs						
Output Voltage						
High				1375	mV	
Low		1025			mV	
Output Differential Voltage		150			mV	Programmable in 75 mV steps
Output Offset Voltage			1200		mV	
GENERAL-PURPOSE OUTPUTS						
Output Voltage						
High		VDD_GPO × 0.8			V	
Low				VDD_GPO × 0.2	V	
Output Current			10		mA	
SPI TIMING						VDD_INTERFACE = 1.8 V
SPI_CLK						
Period	t _{CP}	20			ns	
Pulse Width	t _{MP}	9			ns	
SPI_ENB Setup to First SPI_CLK Rising Edge	t _{SC}	1			ns	
Last SPI_CLK Falling Edge to SPI_ENB Hold	t _{HC}	0			ns	
SPI_DI						
Data Input Setup to SPI_CLK	t _S	2			ns	
Data Input Hold to SPI_CLK	t _H	1			ns	
SPI_CLK Rising Edge to Output Data Delay						
4-Wire Mode	t _{CO}	3		8	ns	
3-Wire Mode	t _{CO}	3		8	ns	
Bus Turnaround Time, Read	t _{HZM}	t _H		t _{CO (max)}	ns	After BBP drives the last address bit
Bus Turnaround Time, Read	t _{HZS}	0		t _{CO (max)}	ns	After MCT9361 drives the last data bit
DIGITAL DATA TIMING (CMOS), VDD_INTERFACE = 1.8 V						
DATA_CLK Clock Period	t _{CP}	16.276			ns	61.44 MHz
DATA_CLK and FB_CLK Pulse Width TX Data	t _{MP}	45% of t _{CP}		55% of t _{CP}	ns	
Setup to FB_CLK	t _{STX}	1			ns	
Hold to FB_CLK	t _{HTX}	0			ns	
DATA_CLK to Data Bus Output Delay	t _{DRX}	0		1.5	ns	
DATA_CLK to RX_FRAME Delay	t _{DDV}	0		1.0	ns	

SPECIFICATIONS

Table 1. (Continued)

Parameter ¹	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
Pulse Width						
ENABLE	t_{ENPW}	t_{CP}			ns	
TXNRX	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent ENSM mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode
Bus Turnaround Time						
Before RX	t_{RPRE}	$2 \times t_{CP}$			ns	TDD mode
After RX	t_{RPST}	$2 \times t_{CP}$			ns	TDD mode
Capacitive Load			3		pF	
Capacitive Input			3		pF	
DIGITAL DATA TIMING (CMOS), VDD_INTERFACE = 2.5 V						
DATA_CLK Clock Period	t_{CP}	16.276			ns	61.44 MHz
DATA_CLK and FB_CLK Pulse Width	t_{MP}	45% of t_{CP}		55% of t_{CP}	ns	
TX Data						TX_FRAME, P0_D, and P1_D
Setup to FB_CLK	t_{STX}	1			ns	
Hold to FB_CLK	t_{HTX}	0			ns	
DATA_CLK to Data Bus Output Delay	t_{DDR}	0		1.2	ns	
DATA_CLK to RX_FRAME Delay	t_{DDV}	0		1.0	ns	
Pulse Width						
ENABLE	t_{ENPW}	t_{CP}			ns	
TXNRX	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent ENSM mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode
Bus Turnaround Time						
Before RX	t_{RPRE}	$2 \times t_{CP}$			ns	TDD mode
After RX	t_{RPST}	$2 \times t_{CP}$			ns	TDD mode
Capacitive Load			3		pF	
Capacitive Input			3		pF	
DIGITAL DATA TIMING (LVDS)						
DATA_CLK Clock Period	t_{CP}	4.069			ns	245.76 MHz
DATA_CLK and FB_CLK Pulse Width	t_{MP}	45% of t_{CP}		55% of t_{CP}	ns	
TX Data						TX_FRAME and TX_D
Setup to FB_CLK	t_{STX}	1			ns	
Hold to FB_CLK	t_{HTX}	0			ns	
DATA_CLK to Data Bus Output Delay	t_{DDR}	0.25		1.25	ns	
DATA_CLK to RX_FRAME Delay	t_{DDV}	0.25		1.25	ns	
Pulse Width						
ENABLE	t_{ENPW}	t_{CP}			ns	
TXNRX	$t_{TXNRXPW}$	t_{CP}			ns	FDD independent ENSM mode
TXNRX Setup to ENABLE	$t_{TXNRXSU}$	0			ns	TDD ENSM mode
Bus Turnaround Time						
Before RX	t_{RPRE}	$2 \times t_{CP}$			ns	
After RX	t_{RPST}	$2 \times t_{CP}$			ns	

SPECIFICATIONS

Table 1. (Continued)

Parameter ¹	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
Capacitive Load			3		pF	
Capacitive Input			3		pF	
SUPPLY CHARACTERISTICS						
1.3 V Main Supply Voltage		1.267	1.3	1.33	V	
VDD_INTERFACE Supply Nominal Settings						
CMOS		1.2		2.5	V	
LVDS		1.8		2.5	V	
VDD_INTERFACE Tolerance		-5		+5	%	Tolerance is applicable to any voltage setting
VDD_GPO Supply Nominal Setting		1.3		3.3	V	When unused, must be set to 1.3 V
VDD_GPO Tolerance		-5		+5	%	Tolerance is applicable to any voltage setting
Current Consumption						
VDDx, Sleep Mode			180		μA	Sum of all input currents
VDD_GPO			50		μA	No load

CURRENT CONSUMPTION—VDD_INTERFACE

Table 2. VDD_INTERFACE = 1.2 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SLEEP MODE		45		μA	Power applied, device disabled
1RX, 1TX, DDR					
LTE10					
Single Port		2.9		mA	30.72 MHz data clock, CMOS
Dual Port		2.7		mA	15.36 MHz data clock, CMOS
LTE20					
Dual Port		5.2		mA	30.72 MHz data clock, CMOS
2RX, 2TX, DDR					
LTE3					
Dual Port		1.3		mA	7.68 MHz data clock, CMOS
LTE10					
Single Port		4.6		mA	61.44 MHz data clock, CMOS
Dual Port		5.0		mA	30.72 MHz data clock, CMOS
LTE20					
Dual Port		8.2		mA	61.44 MHz data clock, CMOS
GSM					
Dual Port		0.2		mA	1.08 MHz data clock, CMOS
WiMAX 8.75					
Dual Port		3.3		mA	20 MHz data clock, CMOS
WiMAX 10					
Single Port					
TDD RX		0.5		mA	22.4 MHz data clock, CMOS
TDD TX		3.6		mA	22.4 MHz data clock, CMOS
FDD		3.8		mA	44.8 MHz data clock, CMOS

SPECIFICATIONS

Table 2. VDD_INTERFACE = 1.2 V (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
WiMAX 20 Dual Port FDD		6.7		mA	44.8 MHz data clock, CMOS

Table 3. VDD_INTERFACE = 1.8 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SLEEP MODE		84		μA	Power applied, device disabled
1RX, 1TX, DDR					
LTE10					
Single Port		4.5		mA	30.72 MHz data clock, CMOS
Dual Port		4.1		mA	15.36 MHz data clock, CMOS
LTE20					
Dual Port		8.0		mA	15.36 MHz data clock, CMOS
2RX, 2TX, DDR					
LTE3					
Dual Port		2.0		mA	7.68 MHz data clock, CMOS
LTE10					
Single Port		8.0		mA	61.44 MHz data clock, CMOS
Dual Port		7.5		mA	30.72 MHz data clock, CMOS
LTE20					
Dual Port		14.0		mA	61.44 MHz data clock, CMOS
GSM					
Dual Port		0.3		mA	1.08 MHz data clock, CMOS
WiMAX 8.75					
Dual Port		5.0		mA	20 MHz data clock, CMOS
WiMAX 10					
Single Port					
TDD RX		0.7		mA	22.4 MHz data clock, CMOS
TDD TX		5.6		mA	22.4 MHz data clock, CMOS
FDD		6.0		mA	44.8 MHz data clock, CMOS
WiMAX 20					
Dual Port					
FDD		10.7		mA	44.8 MHz data clock, CMOS
P-P56					
75 mV Differential Output		14.0		mA	240 MHz data clock, LVDS
300 mV Differential Output		35.0		mA	240 MHz data clock, LVDS
450 mV Differential Output		47.0		mA	240 MHz data clock, LVDS

Table 4. VDD_INTERFACE = 2.5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SLEEP MODE		150		μA	Power applied, device disabled
1RX, 1TX, DDR					
LTE10					
Single Port		6.5		mA	30.72 MHz data clock, CMOS
Dual Port		6.0		mA	15.36 MHz data clock, CMOS
LTE20					
Dual Port		11.5		mA	30.72 MHz data clock, CMOS

SPECIFICATIONS

Table 4. VDD_INTERFACE = 2.5 V (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
2RX, 2TX, DDR					
LTE3					
Dual Port		3.0		mA	7.68 MHz data clock, CMOS
LTE10					
Single Port		11.5		mA	61.44 MHz data clock, CMOS
Dual Port		10.0		mA	30.72 MHz data clock, CMOS
LTE20					
Dual Port		20.0		mA	61.44 MHz data clock, CMOS
GSM					
Dual Port		0.5		mA	1.08 MHz data clock, CMOS
WiMAX 8.75					
Dual Port		7.3		mA	20 MHz data clock, CMOS
WiMAX 10					
Single Port					
TDD RX		1.3		mA	22.4 MHz data clock, CMOS
TDD TX		8.0		mA	22.4 MHz data clock, CMOS
FDD		8.7		mA	44.8 MHz data clock, CMOS
WiMAX 20					
Dual Port					
FDD		15.3		mA	44.8 MHz data clock, CMOS
P-P56					
75 mV Differential Output		26.0		mA	240 MHz data clock, LVDS
300 mV Differential Output		45.0		mA	240 MHz data clock, LVDS
450 mV Differential Output		58.0		mA	240 MHz data clock, LVDS

CURRENT CONSUMPTION—VDDD1P3_DIG AND VDDAX (COMBINATION OF ALL 1.3 V SUPPLIES)

Table 5. 800 MHz, TDD Mode

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX					
5 MHz Bandwidth		180		mA	Continuous RX
10 MHz Bandwidth		210		mA	Continuous RX
20 MHz Bandwidth		260		mA	Continuous RX
2RX					
5 MHz Bandwidth		265		mA	Continuous RX
10 MHz Bandwidth		315		mA	Continuous RX
20 MHz Bandwidth		405		mA	Continuous RX
1TX					
5 MHz Bandwidth					
7 dBm		340		mA	Continuous TX
-27 dBm		190		mA	Continuous TX
10 MHz Bandwidth					
7 dBm		360		mA	Continuous TX
-27 dBm		220		mA	Continuous TX

SPECIFICATIONS

Table 5. 800 MHz, TDD Mode (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
20 MHz Bandwidth					
7 dBm		400		mA	Continuous TX
-27 dBm		250		mA	Continuous TX
2TX					
5 MHz Bandwidth					
7 dBm		550		mA	Continuous TX
-27 dBm		260		mA	Continuous TX
10 MHz Bandwidth					
7 dBm		600		mA	Continuous TX
-27 dBm		310		mA	Continuous TX
20 MHz Bandwidth					
7 dBm		660		mA	Continuous TX
-27 dBm		370		mA	Continuous TX

Table 6. TDD Mode, 2.4 GHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX					
5 MHz Bandwidth		175		mA	Continuous RX
10 MHz Bandwidth		200		mA	Continuous RX
20 MHz Bandwidth		240		mA	Continuous RX
2RX					
5 MHz Bandwidth		260		mA	Continuous RX
10 MHz Bandwidth		305		mA	Continuous RX
20 MHz Bandwidth		390		mA	Continuous RX
1TX					
5 MHz Bandwidth					
7 dBm		350		mA	Continuous TX
-27 dBm		160		mA	Continuous TX
10 MHz Bandwidth					
7 dBm		380		mA	Continuous TX
-27 dBm		220		mA	Continuous TX
20 MHz Bandwidth					
7 dBm		410		mA	Continuous TX
-27 dBm		260		mA	Continuous TX
2TX					
5 MHz Bandwidth					
7 dBm		580		mA	Continuous TX
-27 dBm		280		mA	Continuous TX
10 MHz Bandwidth					
7 dBm		635		mA	Continuous TX
-27 dBm		330		mA	Continuous TX
20 MHz Bandwidth					
7 dBm		690		mA	Continuous TX
-27 dBm		390		mA	Continuous TX

SPECIFICATIONS

Table 7. TDD Mode, 5.5 GHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX					
5 MHz Bandwidth		175		mA	Continuous RX
40 MHz Bandwidth		275		mA	Continuous RX
2RX					
5 MHz Bandwidth		270		mA	Continuous RX
40 MHz Bandwidth		445		mA	Continuous RX
1TX					
5 MHz Bandwidth					
7 dBm		400		mA	Continuous TX
-27 dBm		240		mA	Continuous TX
40 MHz Bandwidth					
7 dBm		490		mA	Continuous TX
-27 dBm		385		mA	Continuous TX
2TX					
5 MHz Bandwidth					
7 dBm		650		mA	Continuous TX
-27 dBm		335		mA	Continuous TX
40 MHz Bandwidth					
7 dBm		820		mA	Continuous TX
-27 dBm		500		mA	Continuous TX

Table 8. FDD Mode, 800 MHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX, 1TX					
5 MHz Bandwidth					
7 dBm		490		mA	
-27 dBm		345		mA	
10 MHz Bandwidth					
7 dBm		540		mA	
-27 dBm		395		mA	
20 MHz Bandwidth					
7 dBm		615		mA	
-27 dBm		470		mA	
2RX, 1TX					
5 MHz Bandwidth					
7 dBm		555		mA	
-27 dBm		410		mA	
10 MHz Bandwidth					
7 dBm		625		mA	
-27 dBm		480		mA	
20 MHz Bandwidth					
7 dBm		740		mA	
-27 dBm		600		mA	

SPECIFICATIONS

Table 8. FDD Mode, 800 MHz (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX, 2TX					
5 MHz Bandwidth					
7 dBm		685		mA	
-27 dBm		395		mA	
10 MHz Bandwidth					
7 dBm		755		mA	
-27 dBm		465		mA	
20 MHz Bandwidth					
7 dBm		850		mA	
-27 dBm		570		mA	
2RX, 2TX					
5 MHz Bandwidth					
7 dBm		790		mA	
-27 dBm		495		mA	
10 MHz Bandwidth					
7 dBm		885		mA	
-27 dBm		590		mA	
20 MHz Bandwidth					
7 dBm		1020		mA	
-27 dBm		730		mA	

Table 9. FDD Mode, 2.4 GHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX, 1TX					
5 MHz Bandwidth					
7 dBm		500		mA	
-27 dBm		350		mA	
10 MHz Bandwidth					
7 dBm		540		mA	
-27 dBm		390		mA	
20 MHz Bandwidth					
7 dBm		620		mA	
-27 dBm		475		mA	
2RX, 1TX					
5 MHz Bandwidth					
7 dBm		590		mA	
-27 dBm		435		mA	
10 MHz Bandwidth					
7 dBm		660		mA	
-27 dBm		510		mA	
20 MHz Bandwidth					
7 dBm		770		mA	
-27 dBm		620		mA	

SPECIFICATIONS

Table 9. FDD Mode, 2.4 GHz (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX, 2TX				mA	
5 MHz Bandwidth					
7 dBm		730		mA	
-27 dBm		425		mA	
10 MHz Bandwidth					
7 dBm		800		mA	
-27dBm		500		mA	
20 MHz Bandwidth					
7 dBm		900		mA	
-27 dBm		600		mA	
2RX, 2TX				mA	
5 MHz Bandwidth					
7 dBm		820			
-27 dBm		515		mA	
10 MHz Bandwidth					
7 dBm		900		mA	
-27 dBm		595		mA	
20 MHz Bandwidth					
7 dBm		1050		mA	
-27 dBm		740		mA	

Table 10. FDD Mode, 5.5 GHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
1RX, 1TX					
5 MHz Bandwidth					
7 dBm		550		mA	
-27 dBm		385		mA	
2RX, 1TX					
5 MHz Bandwidth					
7 dBm		645		mA	
-27 dBm		480		mA	
1RX, 2TX					
5 MHz Bandwidth					
7 dBm		805		mA	
-27 dBm		480		mA	
2RX, 2TX					
5 MHz Bandwidth					
7 dBm		895		mA	
-27 dBm		575		mA	

ABSOLUTE MAXIMUM RATINGS**Table 11.**

Parameter	Rating
VDDx to VSSx	-0.3 V to +1.4 V
VDD_INTERFACE to VSSx	-0.3 V to +3.0 V
VDD_GPO to VSSx	-0.3 V to +3.9 V
Logic Inputs and Outputs to VSSx	-0.3 V to VDD_INTERFACE + 0.3 V
Input Current to Any Pin Except Supplies	±10 mA
RF Inputs (Peak Power)	2.5 dBm
TX Monitor Input Power (Peak Power)	9 dBm
Package Power Dissipation	$(T_{JMAX} - T_A)/\theta_{JA}$
Maximum Junction Temperature(T_{JMAX})	110°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12
A	RX2A_N	RX2A_P	NC	VSSA	TX_MON2	VSSA	TX2A_N	TX2A_P	TX2B_N	TX2B_P	VDDA1P1_TX_VCO	TX_EXT_LO_IN
B	VSSA	VSSA	AUXDAC1	GPO_3	GPO_2	GPO_1	GPO_0	VDD_GPO	VDDA1P3_TX_LO	VDDA1P3_TX_VCO_LDO	TX_VCO_LDO_OUT	VSSA
C	RX2C_P	VSSA	AUXDAC2	TEST/ENABLE	CTRL_IN0	CTRL_IN1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	RX2C_N	VDDA1P3_RX_RF	VDDA1P3_RX_TX	CTRL_OUT0	CTRL_IN3	CTRL_IN2	P0_D9/TX_D4_P	P0_D7/TX_D3_P	P0_D5/TX_D2_P	P0_D3/TX_D1_P	P0_D1/TX_D0_P	VSSD
E	RX2B_P	VDDA1P3_RX_LO	VDDA1P3_TX_LO_BUFFER	CTRL_OUT1	CTRL_OUT2	CTRL_OUT3	P0_D11/TX_D5_P	P0_D8/TX_D4_N	P0_D6/TX_D3_N	P0_D4/TX_D2_N	P0_D2/TX_D1_N	P0_D0/TX_D0_N
F	RX2B_N	VDDA1P3_RX_VCO_LDO	VSSA	CTRL_OUT6	CTRL_OUT5	CTRL_OUT4	VSSD	P0_D10/TX_D5_N	VSSD	FB_CLK_P	VSSD	VDDA1P3_DIG
G	RX_EXT_LO_IN	RX_VCO_LDO_OUT	VDDA1P1_RX_VCO	CTRL_OUT7	EN_AGC	ENABLE	RX_FRAME_N	RX_FRAME_P	TX_FRAME_P	FB_CLK_N	DATA_CLK_P	VSSD
H	RX1B_P	VSSA	VSSA	TXNRX	SYNC_IN	VSSA	VSSD	P1_D11/RX_D5_P	TX_FRAME_N	VSSD	DATA_CLK_N	VDD_INTERFACE
J	RX1B_N	VSSA	VDDA1P3_RX_SYNTH	SPI_DI	SPI_CLK	CLK_OUT	P1_D10/RX_D5_N	P1_D9/RX_D4_P	P1_D7/RX_D3_P	P1_D5/RX_D2_P	P1_D3/RX_D1_P	P1_D1/RX_D0_P
K	RX1C_P	VSSA	VDDA1P3_TX_SYNTH	VDDA1P3_BB	RESETB	SPI_ENB	P1_D8/RX_D4_N	P1_D6/RX_D3_N	P1_D4/RX_D2_N	P1_D2/RX_D1_N	P1_D0/RX_D0_N	VSSD
L	RX1C_N	VSSA	VSSA	RBIAS	AUXADC	SPL_DO	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
M	RX1A_P	RX1A_N	NC	VSSA	TX_MON1	VSSA	TX1A_P	TX1A_N	TX1B_P	TX1B_N	XTALP	XTALN

ANALOG I/O DC POWER
 DIGITAL I/O GROUND
 NO CONNECT

Figure 2. Pin Configuration, Top View

Table 13. Pin Function Descriptions

Pin No.	Type ¹	Mnemonic	Description
A1, A2	I	RX2A_N, RX2A_P	Receive Channel 2 Differential Input A. Alternatively, each pin can be used as a single-ended input or combined to make a differential pair. Tie unused pins to ground.
A3, M3	NC	NC	No Connect. Do not connect to these pins.
A4, A6, B1, B2, B12, C2, C7 to C12, F3, H2, H3, H6, J2, K2, L2, L3, L7 to L12, M4, M6	I	VSSA	Analog Ground. Tie these pins directly to the VSSD digital ground on the printed circuit board (one ground plane).
A5	I	TX_MON2	Transmit Channel 2 Power Monitor Input. If this pin is unused, tie it to ground.
A7, A8	O	TX2A_N, TX2A_P	Transmit Channel 2 Differential Output A. Tie unused pins to 1.3 V.
A9, A10	O	TX2B_N, TX2B_P	Transmit Channel 2 Differential Output B. Tie unused pins to 1.3 V.
A11	I	VDDA1P1_TX_VCO	Transmit VCO Supply Input. Connect to B11.
A12	I	TX_EXT_LO_IN	External Transmit LO Input. If this pin is unused, tie it to ground.
B3	O	AUXDAC1	Auxiliary DAC 1 Output.
B4 to B7	O	GPO_3 to GPO_0	3.3 V Capable General-Purpose Outputs.
B8	I	VDD_GPO	2.5 V to 3.3 V Supply for the AUXDAC and General-Purpose Output Pins. When the VDD_GPO supply is not used, this supply must be set to 1.3 V.
B9	I	VDDA1P3_TX_LO	Transmit LO 1.3 V Supply Input.
B10	I	VDDA1P3_TX_VCO_LDO	Transmit VCO LDO 1.3 V Supply Input. Connect to B9.
B11	O	TX_VCO_LDO_OUT	Transmit VCO LDO Output. Connect to A11 and a 1 μF bypass capacitor in series with a 1 Ω resistor to ground.
C1, D1	I	RX2C_P, RX2C_N	Receive Channel 2 Differential Input C. Each pin can be used as a single-ended input or combined to make a differential pair. These inputs experience degraded performance above 3 GHz. Tie unused pins to ground.
C3	O	AUXDAC2	Auxiliary DAC 2 Output.
C4	I	TEST/ENABLE	Test Input. Ground this pin for normal operation.
C5, C6, D6, D5	I	CTRL_IN0 to CTRL_IN3	Control Inputs. Used for manual RX gain and TX attenuation control.
D2	I	VDDA1P3_RX_RF	Receiver 1.3 V Supply Input. Connect to D3.
D3	I	VDDA1P3_RX_TX	1.3 V Supply Input.
D4, E4 to E6, F4 to F6, G4	O	CTRL_OUT0, CTRL_OUT1 to CTRL_OUT3, CTRL_OUT6 to CTRL_OUT4, CTRL_OUT7	Control Outputs. These pins are multipurpose outputs that have programmable functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

Pin No.	Type ¹	Mnemonic	Description
D7	I/O	P0_D9/TX_D4_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D9, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D4_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D8	I/O	P0_D7/TX_D3_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D7, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D3_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D9	I/O	P0_D5/TX_D2_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D5, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D2_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D10	I/O	P0_D3/TX_D1_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D3, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D1_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D11	I/O	P0_D1/TX_D0_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D1, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D0_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D12, F7, F9, F11, G12, H7, H10, K12	I	VSSD	Digital Ground. Tie these pins directly to the VSSA analog ground on the printed circuit board (one ground plane).
E1, F1	I	RX2B_P, RX2B_N	Receive Channel 2 Differential Input B. Each pin can be used as a single-ended input or combined to make a differential pair. These inputs experience degraded performance above 3 GHz. Tie unused pins to ground.
E2	I	VDDA1P3_RX_LO	Receive LO 1.3 V Supply Input.
E3	I	VDDA1P3_TX_LO_BUFFER	1.3 V Supply Input.
E7	I/O	P0_D11/TX_D5_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D11, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D5_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E8	I/O	P0_D8/TX_D4_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D8, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D4_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E9	I/O	P0_D6/TX_D3_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D6, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D3_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E10	I/O	P0_D4/TX_D2_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D4, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D2_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E11	I/O	P0_D2/TX_D1_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D2, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D1_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E12	I/O	P0_D0/TX_D0_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D0, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D0_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
F2	I	VDDA1P3_RX_VCO_LDO	Receive VCO LDO 1.3 V Supply Input. Connect to E2.
F8	I/O	P0_D10/TX_D5_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D10, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D5_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
F10, G10	I	FB_CLK_P, FB_CLK_N	Feedback Clock. These pins receive the FB_CLK signal that clocks in TX data. In CMOS mode, use FB_CLK_P as the input and tie FB_CLK_N to ground.
F12	I	VDDD1P3_DIG	1.3 V Digital Supply Input.
G1	I	RX_EXT_LO_IN	External Receive LO Input. If this pin is unused, tie it to ground.
G2	O	RX_VCO_LDO_OUT	Receive VCO LDO Output. Connect this pin directly to G3 and a 1 μ F bypass capacitor in series with a 1 Ω resistor to ground.
G3	I	VDDA1P1_RX_VCO	Receive VCO Supply Input. Connect this pin directly to G2 only.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

Pin No.	Type ¹	Mnemonic	Description
G5	I	EN_AGC	Manual Control Input for Automatic Gain Control (AGC).
G6	I	ENABLE	Control Input. This pin moves the device through various operational states.
G7, G8	O	RX_FRAME_N, RX_FRAME_P	Receive Digital Data Framing Output Signal. These pins transmit the RX_FRAME signal that indicates whether the RX output data is valid. In CMOS mode, use RX_FRAME_P as the output and leave RX_FRAME_N unconnected.
G9, H9	I	TX_FRAME_P, TX_FRAME_N	Transmit Digital Data Framing Input Signal. These pins receive the TX_FRAME signal that indicates when TX data is valid. In CMOS mode, use TX_FRAME_P as the input and tie TX_FRAME_N to ground.
G11, H11	O	DATA_CLK_P, DATA_CLK_N	Receive Data Clock Output. These pins transmit the DATA_CLK signal that is used by the BBP to clock RX data. In CMOS mode, use DATA_CLK_P as the output and leave DATA_CLK_N unconnected.
H1, J1	I	RX1B_P, RX1B_N	Receive Channel 1 Differential Input B. Alternatively, each pin can be used as a single-ended input. These inputs experience degraded performance above 3 GHz. Tie unused pins to ground.
H4	I	TXNRX	Enable State Machine Control Signal. This pin controls the data port bus direction. Logic low selects the RX direction, and logic high selects the TX direction.
H5	I	SYNC_IN	Input to Synchronize Digital Clocks Between Multiple MCT9361 Devices. If this pin is unused, tied it to ground.
H8	I/O	P1_D11/RX_D5_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D11, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D5_P) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
H12	I	VDD_INTERFACE	1.2 V to 2.5 V Supply for Digital I/O Pins (1.8 V to 2.5 V in LVDS Mode).
J3	I	VDDA1P3_RX_SYNTH	1.3 V Supply Input.
J4	I	SPI_DI	SPI Serial Data Input.
J5	I	SPI_CLK	SPI Clock Input.
J6	O	CLK_OUT	Output Clock. This pin can be configured to output either a buffered version of the external input clock, the DCXO, or a divided-down version of the internal ADC_CLK.
J7	I/O	P1_D10/RX_D5_N	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D10, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D5_N) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
J8	I/O	P1_D9/RX_D4_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D9, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D4_P) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
J9	I/O	P1_D7/RX_D3_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D7, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D3_P) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
J10	I/O	P1_D5/RX_D2_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D5, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D2_P) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
J11	I/O	P1_D3/RX_D1_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D3, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D1_P) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
J12	I/O	P1_D1/RX_D0_P	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D1, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D0_P) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
K1, L1	I	RX1C_P, RX1C_N	Receive Channel 1 Differential Input C. Alternatively, each pin can be used as a single-ended input. These inputs experience degraded performance above 3 GHz. Tie unused pins to ground.
K3	I	VDDA1P3_TX_SYNTH	1.3 V Supply Input.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

Pin No.	Type ¹	Mnemonic	Description
K4	I	VDDA1P3_BB	1.3 V Supply Input.
K5	I	RESETB	Asynchronous Reset. Logic low resets the device.
K6	I	SPI_ENB	SPI Enable Input. Set this pin to logic low to enable the SPI bus.
K7	I/O	P1_D8/RX_D4_N	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D8, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D4_N) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
K8	I/O	P1_D6/RX_D3_N	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D6, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D3_N) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
K9	I/O	P1_D4/RX_D2_N	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D4, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D2_N) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
K10	I/O	P1_D2/RX_D1_N	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D2, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D1_N) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
K11	I/O	P1_D0/RX_D0_N	Digital Data Port P1/Receive Differential Output Bus. This is a dual function pin. As P1_D0, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D0_N) can function as part of the LVDS 6-bit RX differential output bus with internal LVDS termination.
L4	I	RBIAS	Bias Input Reference. Connect this pin through a 14.3 k Ω (1% tolerance) resistor to ground.
L5	I	AUXADC	Auxiliary ADC Input. If this pin is unused, tie it to ground.
L6	O	SPI_DO	SPI Serial Data Output in 4-Wire Mode, or High-Z in 3-Wire Mode.
M1, M2	I	RX1A_P, RX1A_N	Receive Channel 1 Differential Input A. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground.
M5	I	TX_MON1	Transmit Channel 1 Power Monitor Input. When this pin is unused, tie it to ground.
M7, M8	O	TX1A_P, TX1A_N	Transmit Channel 1 Differential Output A. Tie unused pins to 1.3 V.
M9, M10	O	TX1B_P, TX1B_N	Transmit Channel 1 Differential Output B. Tie unused pins to 1.3 V.
M11, M12	I	XTALP, XTALN	Reference Frequency Crystal Connections. When a crystal is used, connect it between these two pins. When an external clock source is used, connect it to XTALN and leave XTALP unconnected.

THEORY OF OPERATION

GENERAL

The MCT9361 is a highly integrated radio frequency (RF) transceiver capable of being configured for a wide range of applications. The device integrates all RF, mixed signal, and digital blocks necessary to provide all transceiver functions in a single device. Programmability allows this broadband transceiver to be adapted for use with multiple communication standards, including frequency division duplex (FDD) and time division duplex (TDD) systems. This programmability also allows the device to be interfaced to various baseband processors (BBPs) using a single 12-bit parallel data port, dual 12-bit parallel data ports, or a 12-bit low voltage differential signaling (LVDS) interface.

The MCT9361 also provides self-calibration and automatic gain control (AGC) systems to maintain a high performance level under varying temperatures and input signal conditions. In addition, the device includes several test modes that allow system designers to insert test tones and create internal loopback modes that can be used by designers to debug their designs during prototyping and optimize their radio configuration for a specific application.

RECEIVER

The receiver section contains all blocks necessary to receive RF signals and convert them to digital data that is usable by a BBP. There are two independently controlled channels that can receive signals from different sources, allowing the device to be used in multiple input, multiple output (MIMO) systems while sharing a common frequency synthesizer.

Each channel has three inputs that can be multiplexed to the signal chain, making the MCT9361 suitable for use in diversity systems with multiple antenna inputs. The receiver is a direct conversion system that contains a low noise amplifier (LNA), followed by matched in-phase (I) and quadrature (Q) amplifiers, mixers, and band shaping filters that down convert received signals to baseband for digitization. External LNAs can also be interfaced to the device, allowing designers the flexibility to customize the receiver front end for their specific application.

Gain control is achieved by following a preprogrammed gain index map that distributes gain among the blocks for optimal performance at each level. This can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP to make the gain adjustments as needed. Additionally, each channel contains independent RSSI measurement capability, dc offset tracking, and all circuitry necessary for self-calibration.

The receivers include 12-bit, Σ - Δ ADCs and adjustable sample rates that produce data streams from the received signals. The digitized signals can be conditioned further by a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

TRANSMITTER

The transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data received from the BBP passes through a fully programmable 128-tap FIR filter with interpolation options. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both the I and Q channels are fed to the RF block for upconversion.

When converted to baseband analog signals, the I and Q signals are filtered to remove sampling artifacts and fed to the upconversion mixers. At this point, the I and Q signals are recombined and modulated on the carrier frequency for transmission to the output stage. The combined signal also passes through analog filters that provide additional band shaping, and then the signal is transmitted to the output amplifier. Each transmit channel provides a wide attenuation adjustment range with fine granularity to help designers optimize signal-to-noise ratio (SNR).

Self-calibration circuitry is built into each transmit channel to provide automatic real-time adjustment. The transmitter block also provides a TX monitor block for each channel. This block monitors the transmitter output and routes it back through an unused receiver channel to the BBP for signal monitoring. The TX monitor blocks are available only in TDD mode operation while the receiver is idle.

CLOCK INPUT OPTIONS

The MCT9361 operates using a reference clock that can be provided by two different sources. The first option is to use a dedicated crystal with a frequency between 19 MHz and 50 MHz connected between the XTALP and XTALN pins. The second option is to connect an external oscillator or a clock distribution device (such as the AD9548) to the XTALN pin (with the XTALP pin left unconnected). If an external oscillator is used, the frequency can vary between 10 MHz and 80 MHz. This reference clock is used to supply the synthesizer blocks that generate all data clocks, sample clocks, and local oscillators inside the device.

The frequency error of the crystal can be eliminated by adjusting the on-chip variable capacitance using the digitally programmable, digitally controlled crystal oscillator (DCXO) capability. This capacitance can tune the crystal frequency variations in the system, resulting in a more accurate reference clock from which all other frequencies are generated. This feature can also be used in conjunction with the on-chip temperature sensing function to provide temperature compensation of the oscillator frequency during normal operation.

THEORY OF OPERATION

SYNTHESIZERS

RF PLLs

The MCT9361 contains two identical synthesizers to generate the required LO signals for the RF signal paths—one for the receiver and one for the transmitter. Phase-locked loop (PLL) synthesizers are fractional-N designs incorporating completely integrated voltage controlled oscillators (VCOs) and loop filters. In TDD operation, the synthesizers turn on and off as appropriate for the RX and TX frames. In FDD mode, the TX PLL and the RX PLL can be activated simultaneously. These PLLs require no external components.

BB PLL

The MCT9361 also contains a baseband PLL synthesizer that is used to generate all baseband related clock signals. These include the ADC and DAC sampling clocks, the DATA_CLK signal (see the Digital Data Interface section), and all data framing signals. The programming frequency range for this PLL is from 700 MHz to 1400 MHz, depending on the data rate and sample rate requirements of the system.

DIGITAL DATA INTERFACE

The MCT9361 data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP. The data ports can be configured in either single-ended CMOS format or differential LVDS format. Both formats can be configured in multiple arrangements to match system requirements for data ordering and data port connections. These arrangements include single port data bus, dual port data bus, single data rate, double data rate, and various combinations of data ordering to transmit data from different channels across the bus at appropriate times.

Bus transfers are controlled using simple hardware handshake signaling. The two ports can be operated in either bidirectional (TDD) mode or in full duplex (FDD) mode where half the bits are used for transmitting data and half are used for receiving data. The interface can also be configured to use only one of the data ports for applications that do not require high data rates and prefer to use fewer interface pins.

DATA_CLK Signal

RX data supplies the DATA_CLK signal that the BBP can use when receiving the data. The DATA_CLK can be set to a rate that provides single data rate (SDR) timing where data is sampled on each rising clock edge, or it can be set to provide double data rate (DDR) timing where data is captured on both rising and falling edges. This timing applies to operation using either a single port or both ports.

FB_CLK Signal

For transmit data, the interface uses the FB_CLK signal as the

timing reference. The FB_CLK enables source-synchronous timing, aligning with the rising edge for burst control signals and with either the rising edge (in SDR mode) or both edges (in DDR mode) for transmit signal bursts. The FB_CLK signal must have the same frequency and duty cycle as the DATA_CLK.

RX_FRAME Signal

The device generates an RX_FRAME output signal whenever the receiver outputs valid data. This signal has two modes: level mode (RX_FRAME stays high as long as the data is valid) and pulse mode (RX_FRAME pulses with a 50% duty cycle). Similarly, the BBP must provide a TX_FRAME signal that indicates the beginning of a valid data transmission with a rising edge. Similar to the RX_FRAME, the TX_FRAME signal can remain high throughout the burst or it can be pulsed with a 50% duty cycle.

ENABLE STATE MACHINE

The MCT9361 transceiver includes an enable state machine (ENSM) that allows real-time control over the current state of the device. The device can be placed in several different states during normal operation, including

- ▶ Wait—power save, synthesizers disabled
- ▶ Sleep—wait with all clocks/BB PLL disabled
- ▶ TX—TX signal chain enabled
- ▶ RX—RX signal chain enabled
- ▶ FDD—TX and RX signal chains enabled
- ▶ Alert—synthesizers enabled

The ENSM has two possible control methods: SPI control and pin control.

SPI Control Mode

In SPI control mode, the ENSM is controlled asynchronously by writing SPI registers to advance the current state to the next state. SPI control is considered asynchronous to the DATA_CLK because the SPI_CLK can be derived from a different clock reference and can still function properly. The SPI control ENSM method is recommended when real-time control of the synthesizers is not necessary. SPI control can be used for real-time control as long as the BBIC has the ability to perform timed SPI writes accurately.

Pin Control Mode

In pin control mode, the enable function of the ENABLE pin and the TXNRX pin allow real-time control of the current state. The ENSM allows TDD or FDD operation depending on the configuration of the corresponding SPI register. The ENABLE and TXNRX pin control method is recommended if the BBIC has extra control outputs that can be controlled in real time, allowing a simple 2-wire interface to control the state of the device. To advance the current state of the ENSM to the next state, the enable function of the ENABLE pin can be driven by either a pulse (edge detected internally) or a level.

THEORY OF OPERATION

When a pulse is used, it must have a minimum pulse width of one FB_CLK cycle. In level mode, the ENABLE and TXNRX pins are also edge detected by the MCT9361 and must meet the same minimum pulse width requirement of one FB_CLK cycle.

In FDD mode, the ENABLE and TXNRX pins can be remapped to serve as real-time RX and TX data transfer control signals. In this mode, the ENABLE pin enables or disables the receive signal path, and the TXNRX pin enables or disables the transmit signal path. In this mode, the ENSM is removed from the system for control of all data flow by these pins.

SPI INTERFACE

The MCT9361 uses a serial peripheral interface (SPI) to communicate with the BBP. This interface can be configured as a 4-wire interface with dedicated receive and transmit ports, or it can be configured as a 3-wire interface with a bidirectional data communication port. This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol.

Write commands follow a 24-bit format. The first six bits are used to set the bus direction and number of bytes to transfer. The next 10 bits set the address where data is to be written. The final eight bits are the data to be transferred to the specified register address (MSB to LSB). The MCT9361 also supports an LSB-first format that allows the commands to be written in LSB to MSB format. In this mode, the register addresses are incremented for multibyte writes. Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DI pin and the final eight bits are read from the MCT9361, either on the SPI_DO pin in 4-wire mode or on the SPI_DI pin in 3-wire mode.

CONTROL PINS

Control Outputs (CTRL_OUT[7:0])

The MCT9361 provides eight simultaneous real-time output signals for use as interrupts to the BBP. These outputs can be configured to output a number of internal settings and measurements that the BBP can use when monitoring transceiver performance in different situations. The control output pointer register selects what information is output to these pins, and the control output enable register determines which signals are activated for monitoring by the BBP. Signals used for manual gain mode, calibration flags, state machine states, and the ADC output are among the outputs that can be monitored on these pins.

Control Inputs (CTRL_IN[3:0])

The MCT9361 provides four edge detected control input pins. In manual gain mode, the BBP can use these pins to change the gain table index in real time. In transmit mode, the BBP can use two of the pins to change the transmit gain in real time.

GPO PINS (GPO_3 TO GPO_0)

The MCT9361 provides four, 3.3 V capable general-purpose logic output pins: GPO_3, GPO_2, GPO_1, and GPO_0. These pins can be used to control other peripheral devices such as regulators and switches via the MCT9361 SPI bus, or they can function as subordinates for the internal MCT9361 state machine.

AUXILIARY CONVERTERS

AUXADC

The MCT9361 contains an auxiliary ADC that can be used to monitor system functions such as temperature or power output. The converter is 12 bits wide and has an input range of 0 V to 1.25 V. When enabled, the ADC is free running. SPI reads provide the last value latched at the ADC output. A multiplexer in front of the ADC allows the user to select between the AUXADC input pin and a built-in temperature sensor.

AUXDAC1 and AUXDAC2

The MCT9361 contains two identical auxiliary DACs that can provide power amplifier (PA) bias or other system functionality. The auxiliary DACs are 10 bits wide, have an output voltage range of 0.5 V to $VDD_GPO - 0.3$ V, a current drive of 10 mA, and can be directly controlled by the internal enable state machine.

POWERING THE MCT9361

The MCT9361 must be powered by the following three supplies: the analog supply ($VDDD1P3_DIG/VDDAx = 1.3$ V), the interface supply ($VDD_INTERFACE = 1.8$ V), and the GPO supply ($VDD_GPO = 3.3$ V).

PRECAUTIONS

PRODUCTION INSTALLATION

- ▶ Ensure correct orientation during soldering.
- ▶ All debugging instruments and equipment must share a common, high-quality ground. PCB designs must ensure excellent grounding and adequate power supply decoupling.
- ▶ Avoid reverse power connection and short circuits between power supply and input/output pins, as this may cause permanent damage.
- ▶ Electrical Assembly Instructions

This product has a Moisture Sensitivity Level (MSL) of 3. The allowable floor life after removing the product from the moisture barrier bag, after dry storage or baking, until reflow soldering is $\leq 30^{\circ}\text{C}/60\%$ RH, 168 hours. If the storage conditions of the device cannot be controlled or tracked, strictly execute baking at 125°C for 8 hours before electrical assembly. If the temperature and humidity of the electrical assembly environment cannot be guaranteed to be $\leq 30^{\circ}\text{C}/60\%$ RH, complete soldering within 12 hours after baking. After baking, the product is highly prone to electrostatic discharge (ESD), so ESD protection precautions are necessary during all handling processes.

For board-level assembly using leaded reflow soldering (Sn63Pb37), the recommended peak temperature range is $210^{\circ}\text{C}\sim 235^{\circ}\text{C}$, and the maximum peak temperature should not exceed 235°C . The dwell time within $\pm 5^{\circ}\text{C}$ of the peak temperature is $\leq 20\text{s}$, the time above liquidus is 60~90s, the ramp-up rate is $2\sim 4^{\circ}\text{C}/\text{s}$, and the ramp-down rate is $2\sim 6^{\circ}\text{C}/\text{s}$.

For board-level assembly using lead-free reflow soldering (SAC305), the recommended peak temperature range is $230^{\circ}\text{C}\sim 245^{\circ}\text{C}$, and the maximum peak temperature should not exceed 260°C . The dwell time within $\pm 5^{\circ}\text{C}$ of the peak temperature is $\leq 20\text{s}$, the time above liquidus is 60~90s, the ramp-up rate is $2\sim 4^{\circ}\text{C}/\text{s}$, and the ramp-down rate is $2\sim 6^{\circ}\text{C}/\text{s}$.

If mixed electrical assembly processes require higher temperatures, ensure the maximum device body temperature does not exceed 260°C (the measurement point for device body temperature is located on the upper surface of the device during reflow soldering).

PRODUCT USAGE

- ▶ Power-up Sequence: It is recommended to power up the analog and digital supplies simultaneously, or power up the analog supply first.
- ▶ Use capacitors with low ESR for decoupling at the LDO output.
- ▶ In application, it is recommended to use a large-area ground plane on the PCB. This helps eliminate potential differences due to different ground points and also reduces the impact of parasitic capacitance generated by the circuit board on the circuit.
- ▶ Each power supply pin should have a $1\mu\text{F}$ or $0.1\mu\text{F}$ capacitor placed close to it.
- ▶ For the analog input section, if differential input is used, the traces of the differential input pair must be matched in length.
- ▶ Digital and analog power supplies need to be separated.

PRODUCT PROTECTION

All leads of this circuit are designed with electrostatic protection structures. However, high-energy electrical pulses can still potentially damage the circuit. Therefore, electrostatic protection precautions should be observed during testing, handling, and storage.

Note: For more detailed information, please contact the chip designer for technical support.

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

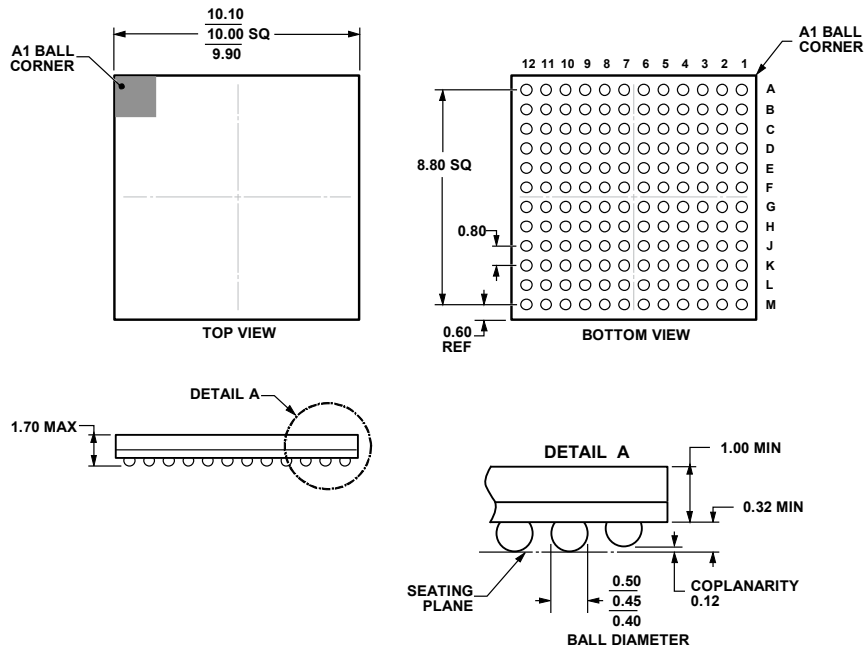


Figure 3. 144-pin BGA package illustration
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Packing Quantity
MCT9361BA	-40°C to +85°C	144-BGA (10mm×10mm)	184/TRAY

MCT9361 and AD9361 Register Configuration Differences

After the user calculates and writes the values for the following two registers, it is necessary to write 0 to the D0 bit of these two registers.

Register Address 0x0D6, D[0] needs to be configured to 0, as shown in the figure below:

TX BBF TUNER CONFIGURATION REGISTERS 0D6 THROUGH 0D7

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
0D6	TX BBF Tune Divider	TX BBF Tune Divider<7:0>							needs be configured to 0	12h	R/W
0D7	TX BBF Tune Mode	Open			EvaTime	Tuner Mode<2:0>		TX BBF Tune Divider<8>		1Ah	R/W

Register Address 0x1F8, D[0] needs to be configured to 0, as shown in the figure below:

RX BBF TUNER CONFIGURATION REGISTERS 1F8 THROUGH 1FC

Register Address	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default	R/W
1F8	RX BBF Tune Divider	RX BBF Tune Divider<7:0>							needs be configured to 0	14h	R/W