1 GSPS, 14-Bit, 3.3 V CMOS Direct Digital Synthesizer

Data Sheet

MCDS9910

FEATURES

1 GSPS internal clock speed (up to 400 MHz analog output)
Integrated 1 GSPS, 14-bit DAC
0.23 Hz or better frequency resolution
Phase noise ≤ −125 dBc/Hz @ 1 kHz offset (400 MHz carrier)
Excellent dynamic performance with
>80 dB narrow-band SFDR
Serial input/output (I/O) control
Automatic linear or arbitrary frequency, phase, and amplitude sweep capability
8 frequency and phase offset profiles
Sin(x)/(x) correction (inverse sinc filter)
1.8 V and 3.3 V power supplies
Software and hardware controlled power-down
100-lead TQFP_EP package
Integrated 1024 word × 32-bit RAM
PLL REFCLK multiplier
Parallel datapath interface
Internal oscillator can be driven by a single crystal
Phase modulation capability
Amplitude modulation capability
Multichip synchronization

APPLICATIONS

Agile local oscillator (LO) frequency synthesis
Programmable clock generators
FM chirp source for radar and scanning systems
Test and measurement equipment
Acousto-optic device drivers
Polar modulators
Fast frequency hopping

GENERAL DESCRIPTION

The MCDS9910 is a direct digital synthesizer (DDS)featuring an integrated 14-bit DAC and supporting sample rates up to 1 GSPS,can generate 400MHz sine waveform.The user has access to the three signal control parameters that control the DDS: frequency, phase, and amplitude.The DDS provides fast frequency hopping and frequency tuning resolution with its 32-bit accumulator. With a 1 GSPS sample rate, the tuning resolution is ~0.23 Hz. The DDS also enables fast phase and amplitude switching capability.The MCDS9910 is controlled by programming its internal control registers via a serial I/O port.The MCDS9910 includes an integrated static RAM to support various combinations of frequency, phase,and/or amplitude modulation. The MCDS9910 also supports a user defined, digitally controlled, digital ramp mode of operation. In this mode, the frequency, phase, or amplitude can be varied linearly over time.For more advanced modulation functions, a high speed parallel data input port is included to enable direct frequency, phase, amplitude, or polar modulation.

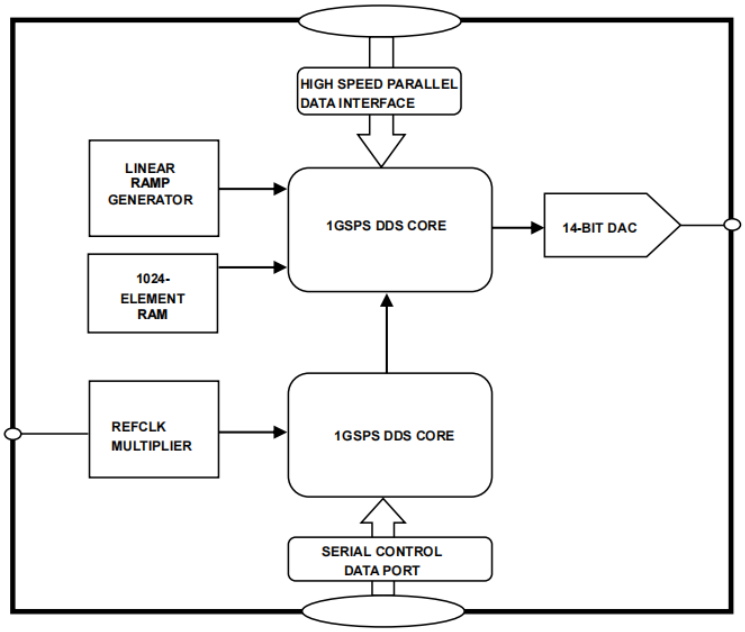


Figure 1.
FUNCTIONAL BLOCK DIAGRAM

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

AVDD (1.8 V) and DVDD (1.8 V) = 1.8 V ± 5%, AVDD (3.3 V) = 3.3 V ± 5%, DVDD_I/O (3.3 V) = 3.3 V ± 5%, T = 25°C, R_{SET} = 10 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 1000 MHz with reference clock (REFCLK) multiplier disabled, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
REFCLK INPUT CHARACTERISTICS					
Frequency Range					
REFCLK Multiplier	Disabled	60		1000	MHz
	Enabled	3.2		60	MHz
Maximum REFCLK Input Divider Frequency	Full temperature range	1500	1900		MHz
Minimum REFCLK Input Divider Frequency	Full temperature range		25	35	MHz
External Crystal			25		MHz
Input Capacitance			3		pF
Input Impedance	Differential		2.8		kΩ
	Single-ended		1.4		kΩ
Duty Cycle	REFCLK multiplier disabled	45		55	%
	REFCLK multiplier enabled	40		60	%
REFCLK Input Level	Single-ended	50		1000	mV p-p
	Differential	100		2000	mV p-p
REFCLK MULTIPLIER VCO CHARACTERISTICS					
VCO Gain (K_V) @ Center Frequency	VCO range Setting 0		429		MHz/V
	VCO range Setting 1		500		MHz/V
	VCO range Setting 2		555		MHz/V
	VCO range Setting 3		750		MHz/V
	VCO range Setting 4		789		MHz/V
	VCO range Setting 5[1]		850		MHz/V
REFCLK_OUT CHARACTERISTICS					
Maximum Capacitive Load			20		pF
Maximum Frequency			25		MHz
DAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current		8.6	20	31.6	mA
Gain Error		−10		+10	% FS
Output Offset				2.3	µA
Differential Nonlinearity			0.8		LSB
Integral Nonlinearity			1.5		LSB
Output Capacitance			5		pF
Residual Phase Noise	@ 1 kHz offset, 20 MHz A_{OUT}				
REFCLK Multiplier	Disabled		−152		dBc/Hz
	Enabled @ 20×		−140		dBc/Hz
	Enabled @ 100×		−140		dBc/Hz
Voltage Compliance Range		−0.5		+0.5	V
Wideband SFDR	See the Typical Performance Characteristics section				
Narrow-Band SFDR					
50.1 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−96		dBc
101.3 MHz Analog Output	±500 kHz		−87		dBc
	±125 kHz		−87		dBc
	±12.5 kHz		−95		dBc

Parameter	Conditions/Comments	Min	Typ	Max	Unit
201.1 MHz Analog Output	±500 kHz		–87		dBc
	±125 kHz		–87		dBc
	±12.5 kHz		–91		dBc
301.1 MHz Analog Output	±500 kHz		–86		dBc
	±125 kHz		–86		dBc
	±12.5 kHz		–88		dBc
401.3 MHz Analog Output	±500 kHz		–84		dBc
	±125 kHz		–84		dBc
	±12.5 kHz		–85		dBc
SERIAL PORT TIMING CHARACTERISTICS					
Maximum SCLK Frequency			70		Mbps
Minimum SCLK Clock Pulse Width	Low	4			ns
	High	4			ns
Maximum SCLK Rise/Fall Time			2		ns
Minimum Data Setup Time to SCLK		5			ns
Minimum Data Hold Time to SCLK		0			ns
Maximum Data Valid Time in Read Mode				11	ns
I/O_UPDATE/PROFILE[2:0] TIMING CHARACTERISTICS					
Minimum Setup Time to SYNC_CLK		1.75			ns
Minimum Hold Time to SYNC_CLK		0			ns
I/O_UPDATE Pulse Width	High	>1			SYNC_CLK cycle
Minimum Profile Toggle Period		2			SYNC_CLK cycles
TxENABLE and 16-BIT PARALLEL (DATA) BUS TIMING					
Maximum PDCLK Frequency			250		MHz
TxENABLE/Data Setup Time (to PDCLK)		1.75			ns
TxENABLE/Data Hold Time (to PDCLK)		0			ns
MISCELLANEOUS TIMING CHARACTERISTICS					
Wake-Up Time[2]					
Fast Recovery			8		SYSCLK cycles[3]
Full Sleep Mode	REFCLK multiplier enabled		1		ms
	REFCLK multiplier disabled			150	µs
Minimum Reset Pulse Width High			5		SYSCLK cycles[3]
DATA LATENCY (PIPELINE DELAY)					
Data Latency, Single Tone or Using Profiles					
Frequency, Phase, Amplitude-to-DAC Output	Matched latency enabled and OSK enabled		91		SYSCLK cycles[3]
Frequency, Phase-to-DAC Output	Matched latency enabled and OSK disabled		79		SYSCLK cycles[3]
	Matched latency disabled		79		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency disabled		47		SYSCLK cycles[3]
Data Latency Using RAM Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		94		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency enabled		106		SYSCLK cycles[3]
	Matched latency disabled		58		SYSCLK cycles[3]
Data Latency, Sweep Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled/disabled		91		SYSCLK cycles[3]
Amplitude-to-DAC Output	Matched latency enabled		91		SYSCLK cycles[3]
	Matched latency disabled		47		SYSCLK cycles[3]
Data Latency, 16-Bit Input Modulation Mode					
Frequency, Phase-to-DAC Output	Matched latency enabled		103		SYSCLK cycles[3]
	Matched latency disabled		91		SYSCLK cycles[3]

Parameter	Conditions/Comments	Min	Typ	Max	Unit
CMOS LOGIC INPUTS					
Logic 1 Voltage		2.0			V
Logic 0 Voltage				0.8	V
Logic 1 Current			90	150	µA
Logic 0 Current			90	150	µA
Input Capacitance			2		pF
XTAL_SEL INPUT					
Logic 1 Voltage		1.25			V
Logic 0 Voltage				0.6	V
Input Capacitance			2		pF
CMOS LOGIC OUTPUTS	1 mA load				
Logic 1 Voltage		2.8			V
Logic 0 Voltage				0.4	V
POWER SUPPLY CURRENT					
I_{AVDD} (1.8 V)			110		mA
I_{AVDD} (3.3 V)			29		mA
I_{DVDD} (1.8 V)			222		mA
I_{DVDD} (3.3 V)			11		mA
TOTAL POWER CONSUMPTION					
Single Tone Mode			715	950	mW
Rapid Power-Down Mode			330	450	mW
Full Sleep Mode			19	40	mW

[1] The gain value for VCO range Setting 5 is measured at 1000 MHz.
[2] Wake-up time refers to the recovery time from a power-down state. The longest time required is for the reference clock multiplier PLL to relock to the reference. The wake-up time assumes that the recommended PLL loop filter values are used.
[3] SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier is not used, the SYSCLK frequency is the same as the external reference clock frequency.

ABSOLUTE MAXIMUM RATINGS

Table 2.

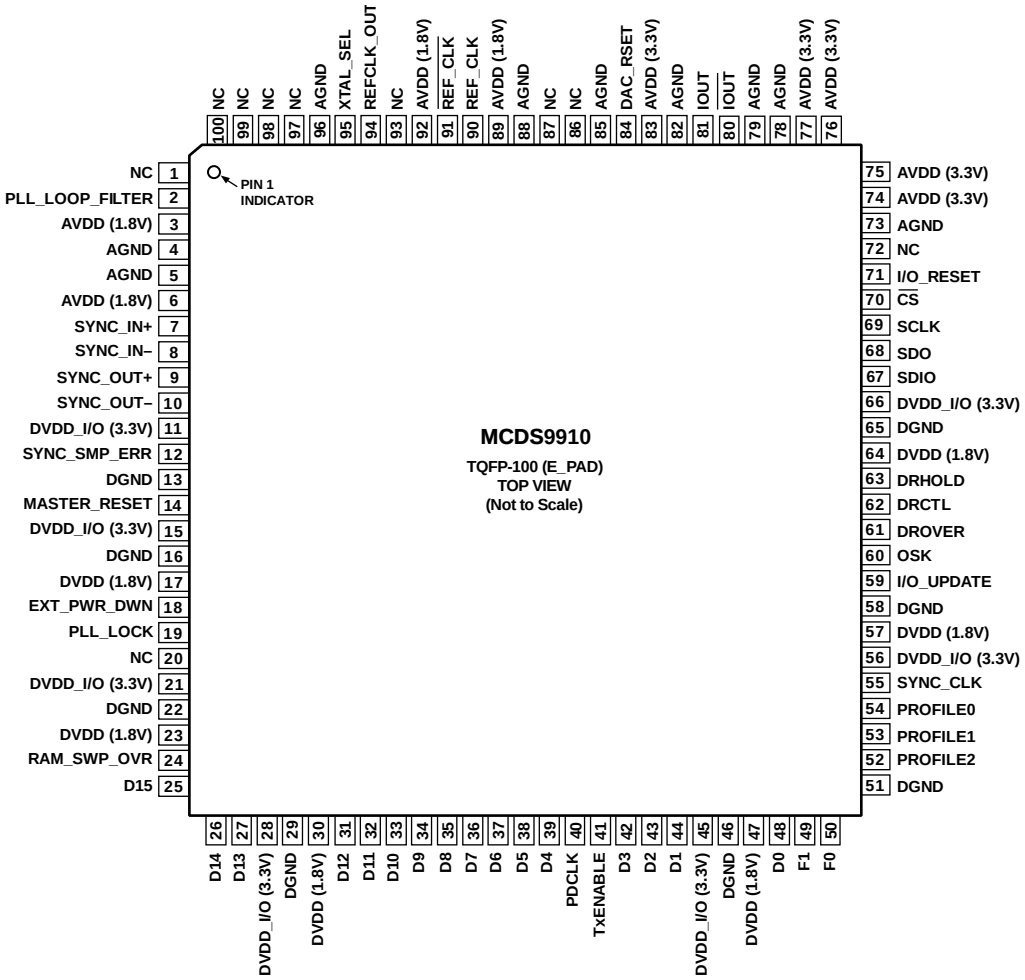
Parameter	Rating
AVDD (1.8V), DVDD (1.8V) Supplies	2 V
AVDD (3.3V), DVDD_I/O (3.3V) Supplies	4 V
Digital Input Voltage	−0.7 V to +4 V
Digital Output Current	5 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
θ_{JA}	22°C/W
θ_{JC}	2.8°C/W
Maximum Junction Temperature	150°C
Lead Temperature (10 sec Soldering)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES:
1. EXPOSED PAD SHOULD BE SOLDERED TO GROUND.
2. NC = NO CONNECT.

Figure 2 . Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1, 20, 72, 86, 87, 93, 97 to 100	NC		Not Connected. Allow device pins to float.
2	PLL_LOOP_FILTER	I	PLL Loop Filter Compensation Pin. See the External PLL Loop Filter Components section for details.
3, 6, 89, 92	AVDD (1.8V)	I	Analog Core VDD, 1.8 V Analog Supplies.
74 to 77, 83	AVDD (3.3V)	I	Analog DAC VDD, 3.3 V Analog Supplies.
17, 23, 30, 47, 57, 64	DVDD (1.8V)	I	Digital Core VDD, 1.8 V Digital Supplies.
11, 15, 21, 28, 45, 56, 66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD, 3.3 V Digital Supplies.
4, 5, 73, 78, 79, 82, 85, 88, 96	AGND	I	Analog Ground.
13, 16, 22, 29, 46, 51, 58, 65	DGND	I	Digital Ground.
7	SYNC_IN+	I	Synchronization Signal (LVDS), Digital Input (Rising Edge Active). The synchronization signal from the external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section for details.
8	SYNC_IN–	I	Synchronization Signal (LVDS), Digital Input. The synchronization signal from the external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section for details.
9	SYNC_OUT+	O	Synchronization Signal (LVDS), Digital Output (Rising Edge Active). The synchronization signal from the internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section for details.
10	SYNC_OUT–	O	Synchronization Signal (LVDS), Digital Output. The synchronization signal from the internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section for details.
12	SYNC_SMP_ERR	O	Synchronization Sample Error, Digital Output (Active High). Sync sample error: a high on this pin indicates that the AD9910 did not receive a valid sync signal on SYNC_IN+/SYNC_IN–.
14	MASTER_RESET	I	Master Reset, Digital Input (Active High). Master reset: clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Control section for further details. If unused, connect to ground.
19	PLL_LOCK	O	Clock Multiplier PLL Lock, Digital Output (Active High). A high on this pin indicates that the Clock Multiplier PLL has acquired lock to the reference clock input.
24	RAM_SWP_OVR	O	RAM Sweep Over, Digital Output (Active High). A high on this pin indicates that the RAM sweep profile has completed.
25 to 27, 31 to 39, 42 to 44, 48	D[15:0]	I	Parallel Input Bus (Active High).
49, 50	F[1:0]	I	Modulation Format Pins. Digital input to determine the modulation format.
40	PDCLK	O	Parallel Data Clock. This is the digital output (clock). The parallel data clock provides a timing signal for aligning data at the parallel inputs.
41	TxENABLE	I	Transmit Enable. Digital input (active high). In burst mode communications, a high on this pin indicates new data for transmission. In continuous mode, this pin remains high.
52 to 54	PROFILE[2:0]	I	Profile Select Pins. Digital inputs (active high). Use these pins to select one of eight phase/frequency profiles for the DDS. Changing the state of one of these pins transfers the current contents of all I/O buffers to the corresponding registers. State changes should be set up on the SYNC_CLK pin.
55	SYNC_CLK	O	Output Clock Divided-By-Four. A digital output (clock). Many of the digital inputs on the chip, such as I/O_UPDATE and PROFILE[2:0], need to be set up on the rising edge of this signal.

Pin No.	Mnemonic	I/O[1]	Description
59	I/O_UPDATE	I/O	Input/Output Update. Digital input (active high). A high on this pin transfers the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Output Shift Keying. Digital input (active high). When the OSK features are placed in either manual or automatic mode, this pin controls the OSK function. In manual mode, it toggles the multiplier between 0 (low) and the programmed amplitude scale factor (high). In automatic mode, a low sweeps the amplitude down to zero, a high sweeps the amplitude up to the amplitude scale factor.
61	DROVER	O	Digital Ramp Over. Digital output (active high). This pin switches to Logic 1 whenever the digital ramp generator reaches its programmed upper or lower limit.
62	DRCTL	I	Digital Ramp Control. Digital input (active high). This pin controls the slope polarity of the digital ramp generator. See the Digital Ramp Generator (DRG) section for more details. If not using the digital ramp generator, connect this pin to Logic 0.
63	DRHOLD	I	Digital Ramp Hold. Digital input (active high). This pin stalls the digital ramp generator in its present state. See the Digital Ramp Generator (DRG) section for more details. If not using a digital ramp generator, connect this pin to Logic 0.
67	SDIO	I/O	Serial Data Input/Output. Digital input/output (active high). This pin can be either unidirectional or bidirectional (default), depending on the configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional mode, it is an input only.
68	SDO	O	Serial Data Output. Digital output (active high). This pin is only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and should be left floating.
69	SCLK	I	Serial Data Clock. Digital clock (rising edge on write, falling edge on read). This pin provides the serial data clock for the control data path. Write operations to the AD9910 use the rising edge. Readback operations from the AD9910 use the falling edge.
70	$\overline{CS}$	I	Chip Select. Digital input (active low). This pin allows the AD9910 to operate on a common serial bus for the control data path. Bringing this pin low enables the AD9910 to detect serial clock rising/falling edges. Bringing this pin high causes the AD9910 to ignore input on the serial data pins.
71	I/O_RESET	I	Input/Output Reset. Digital input (active high). This pin can be used when a serial I/O communication cycle fails (see the I/O_RESET—Input/Output Reset section for details). When not used, connect this pin to ground.
80	$\overline{IOUT}$	O	Open-Drain DAC Complementary Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
81	IOUT	O	Open-Drain DAC Output Source. Analog output (current mode). Connect through a 50 Ω resistor to AGND.
84	DAC_RSET	O	Analog Reference Pin. This pin programs the DAC output full-scale reference current. Attach a 10 kΩ resistor to AGND.
90	REF_CLK	I	Reference Clock Input. Analog input. When the internal oscillator is engaged, this pin can be driven by either an external oscillator or connected to a crystal. See the REF_CLK/ Overview section for more details.
91	$\overline{REF\_CLK}$	I	Reference Clock Input. Analog input. See the REF_CLK/ Overview section for more details.
94	REFCLK_OUT	O	Crystal Output. Analog output. See the REF_CLK/ Overview section for more details.
95	XTAL_SEL	I	Crystal Select (1.8 V Logic). Analog input (active high). Driving the XTAL_SEL pin high, the AVDD (1.8V) pin enables the internal oscillator to be used with a crystal resonator. If unused, connect it to AGND.
EPAD	Exposed Paddle (EPAD)		The EPAD should be soldered to ground.

[1] I = input, O = output.

SERIAL I/O TIMING DIAGRAMS

Figure 3 through Figure 6 provide basic examples of the timing relationships between the various control signals of the serial I/O port . I/O port. Most of the bits in the register map are not transferred to their internal destinations until assertion of an I/O update, which is not included in the timing diagrams that follow.

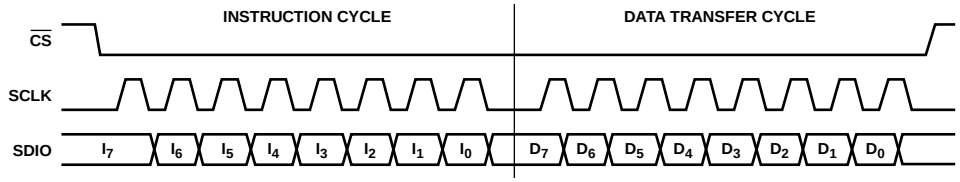


Figure 3. Serial Port Write Timing, Clock Stall Low

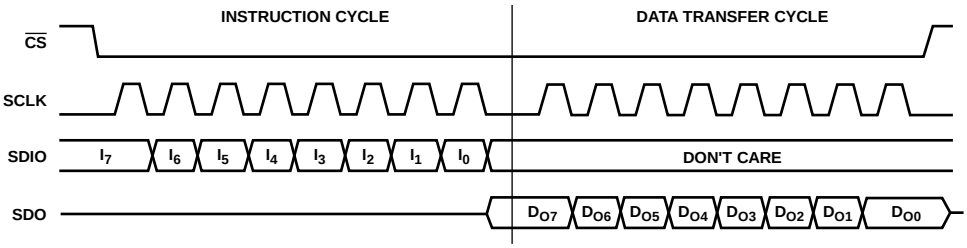


Figure 4. 3-Wire Serial Port Read Timing, Clock Stall Low

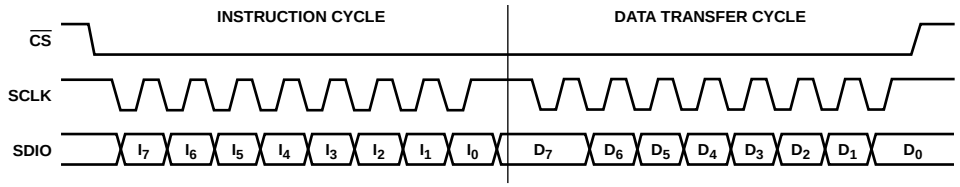


Figure 5. Serial Port Write Timing, Clock Stall High

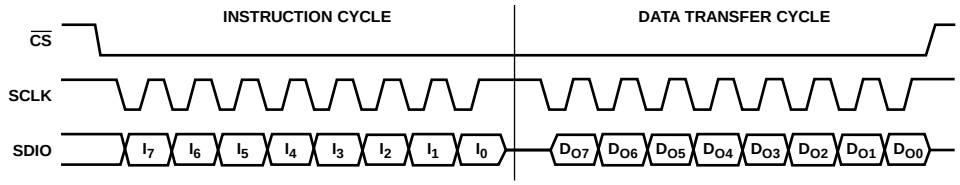


Figure 6. 2-Wire Serial Port Read Timing, Clock Stall High

REGISTER MAP AND BIT DESCRIPTIONS

Table 4. Register Map

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value[1] (Hex)
CFR1—Control Function Register 1 (0x00)	31:24	RAM enable	RAM playback destination		Open					0x00
	23:16	Manual OSK external control	Inverse sinc filter enable	Open	Internal profile control				Select DDS sine output	0x00
	15:8	Load LRR @ I/O update	Autoclear digital ramp accumulator	Autoclear phase accumulator	Clear digital ramp accumulator	Clear phase accumulator	Load ARR @ I/O update	OSK enable	Select auto OSK	0x00
	7:0	Digital power-down	DAC power-down	REFCLK input power-down	Aux DAC power-down	External power-down control	Open	SDIO input only	LSB first	0x00
CFR2—Control Function Register 2 (0x01)	31:24	Open							Enable amplitude scale from single tone profiles	0x00
	23:16	Internal I/O update active	SYNC_CLK enable	Digital ramp destination		Digital ramp enable	Digital ramp no-dwell high	Digital ramp no-dwell low	Read effective FTW	0x40
	15:8	I/O update rate control		Open		PDCLK enable	PDCLK invert	TxEnable invert	Open	0x08
	7:0	Matched latency enable	Data assembler hold last value	Sync timing validation disable	Parallel data port enable	FM gain				0x20
CFR3—Control Function Register 3 (0x02)	31:24	Open		DRV0[1:0]		Open	VCO SEL[2:0]			0x1F
	23:16	Open		I_{CP}[2:0]			Open			0x3F
	15:8	REFCLK input divider bypass	REFCLK input divider ResetB	Open			PFD reset	Open	PLL enable	0x40
	7:0	N[6:0]							Open	0x00
Auxiliary DAC Control (0x03)	31:24	Open								0x00
	23:16	Open								0x00
	15:8	Open								0x00
	7:0	FSC[7:0]								0x7F
I/O Update Rate (0x04)	31:24	I/O update rate[31:24]								0xFF
	23:16	I/O update rate[23:16]								0xFF
	15:8	I/O update rate[15:8]								0xFF
	7:0	I/O update rate[7:0]								0xFF
FTW—Frequency Tuning Word (0x07)	31:24	Frequency tuning word[31:24]								0x00
	23:16	Frequency tuning word[23:16]								0x00
	15:8	Frequency tuning word[15:8]								0x00
	7:0	Frequency tuning word[7:0]								0x00

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value[1] (Hex)
POW—Phase Offset Word (0x08)	15:8	Phase offset word[15:8]								0x00
	7:0	Phase offset word[7:0]								0x00
ASF—Amplitude Scale Factor (0x09)	31:24	Amplitude ramp rate[15:8]								0x00
	23:16	Amplitude ramp rate[7:0]								0x00
	15:8	Amplitude scale factor[13:6]								0x00
	7:0	Amplitude scale factor[5:0]						Amplitude step size[1:0]		0x00
Multichip Sync (0x0A)	31:24	Sync validation delay[3:0]				Sync receiver enable	Sync generator enable	Sync generator polarity	Open	0x00
	23:16	Sync state preset value[5:0]						Open		0x00
	15:8	Output sync generator delay[4:0]					Open			0x00
	7:0	Input sync receiver delay[4:0]					Open			0x00
Digital Ramp Limit (0x0B)	63:56	Digital ramp upper limit[31:24]								N/A
	55:48	Digital ramp upper limit[23:16]								N/A
	47:40	Digital ramp upper limit[15:8]								N/A
	39:32	Digital ramp upper limit[7:0]								N/A
	31:24	Digital ramp lower limit[31:24]								N/A
	23:16	Digital ramp lower limit[23:16]								N/A
	15:8	Digital ramp lower limit[15:8]								N/A
	7:0	Digital ramp lower limit[7:0]								N/A
Digital Ramp Step Size (0x0C)	63:56	Digital ramp decrement step size[31:24]								N/A
	55:48	Digital ramp decrement step size[23:16]								N/A
	47:40	Digital ramp decrement step size[15:8]								N/A
	39:32	Digital ramp decrement step size[7:0]								N/A
	31:24	Digital ramp increment step size[31:24]								N/A
	23:16	Digital ramp increment step size[23:16]								N/A
	15:8	Digital ramp increment step size[15:8]								N/A
	7:0	Digital ramp increment step size[7:0]								N/A
Digital Ramp Rate (0x0D)	31:24	Digital ramp negative slope rate [15:8]								N/A
	23:16	Digital ramp negative slope rate[7:0]								N/A
	15:8	Digital ramp positive slope rate[15:8]								N/A
	7:0	Digital ramp positive slope rate[7:0]								N/A
Single Tone Profile 0 (0x0E)	63:56	Open		Amplitude Scale Factor 0[13:8]						0x08
	55:48	Amplitude Scale Factor 0[7:0]								0xB5
	47:40	Phase Offset Word 0[15:8]								0x00
	39:32	Phase Offset Word 0[7:0]								0x00
	31:24	Frequency Tuning Word 0[31:24]								0x00
	23:16	Frequency Tuning Word 0[23:16]								0x00
	15:8	Frequency Tuning Word 0[15:8]								0x00
	7:0	Frequency Tuning Word 0[7:0]								0x00

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value[1] (Hex)
RAM Profile 0 (0x0E)	63:56	Open								0x00
	55:48	RAM Profile 0 address step rate[15:8]								0x00
	47:40	RAM Profile 0 address step rate[7:0]								0x00
	39:32	RAM Profile 0 waveform end address[9:2]								0x00
	31:24	RAM Profile 0 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 0 waveform start address[9:2]								0x00
	15:8	RAM Profile 0 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 0 mode control[2:0]			0x00
Single Tone Profile 1 (0x0F)	63:56	Open		Amplitude Scale Factor 1[13:8]						0x00
	55:48	Amplitude Scale Factor 1[7:0]								0x00
	47:40	Phase Offset Word 1[15:8]								0x00
	39:32	Phase Offset Word 1[7:0]								0x00
	31:24	Frequency Tuning Word 1[31:24]								0x00
	23:16	Frequency Tuning Word 1[23:16]								0x00
	15:8	Frequency Tuning Word 1[15:8]								0x00
	7:0	Frequency Tuning Word 1[7:0]								0x00
RAM Profile 1 (0x0F)	63:56	Open								0x00
	55:48	RAM Profile 1 address step rate[15:8]								0x00
	47:40	RAM Profile 1 address step rate[7:0]								0x00
	39:32	RAM Profile 1 waveform end address[9:2]								0x00
	31:24	RAM Profile 1 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 1 waveform start address[9:2]								0x00
	15:8	RAM Profile 1 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 1 mode control[2:0]			0x00
Single Tone Profile 2 (0x10)	63:56	Open		Amplitude Scale Factor 2[13:8]						0x00
	55:48	Amplitude Scale Factor 2[7:0]								0x00
	47:40	Phase Offset Word 2[15:8]								0x00
	39:32	Phase Offset Word 2[7:0]								0x00
	31:24	Frequency Tuning Word 2[31:24]								0x00
	23:16	Frequency Tuning Word 2[23:16]								0x00
	15:8	Frequency Tuning Word 2[15:8]								0x00
	7:0	Frequency Tuning Word 2[7:0]								0x00
RAM Profile 2 (0x10)	63:56	Open								0x00
	55:48	RAM Profile 2 address step rate[15:8]								0x00
	47:40	RAM Profile 2 address step rate[7:0]								0x00
	39:32	RAM Profile 2 waveform end address[9:2]								0x00
	31:24	RAM Profile 2 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 2 waveform start address[9:2]								0x00
	15:8	RAM Profile 2 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 2 mode control[2:0]			0x00

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value[1] (Hex)
Single Tone Profile 3 (0x11)	63:56	Open		Amplitude Scale Factor 3[13:8]						0x00
	55:48	Amplitude Scale Factor 3[7:0]								0x00
	47:40	Phase Offset Word 3[15:8]								0x00
	39:32	Phase Offset Word 3[7:0]								0x00
	31:24	Frequency Tuning Word 3[31:24]								0x00
	23:16	Frequency Tuning Word 3[23:16]								0x00
	15:8	Frequency Tuning Word 3[15:8]								0x00
	7:0	Frequency Tuning Word 3[7:0]								0x00
RAM Profile 3 (0x11)	63:56	Open								0x00
	55:48	RAM Profile 3 address step rate[15:8]								0x00
	47:40	RAM Profile 3 address step rate[7:0]								0x00
	39:32	RAM Profile 3 waveform end address[9:2]								0x00
	31:24	RAM Profile 3 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 3 waveform start address[9:2]								0x00
	15:8	RAM Profile 3 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 3 mode control[2:0]			0x00
Single Tone Profile 4 (0x12)	63:56	Open		Amplitude Scale Factor 4[13:8]						0x00
	55:48	Amplitude Scale Factor 4[7:0]								0x00
	47:40	Phase Offset Word 4[15:8]								0x00
	39:32	Phase Offset Word 4[7:0]								0x00
	31:24	Frequency Tuning Word 4[31:24]								0x00
	23:16	Frequency Tuning Word 4[23:16]								0x00
	15:8	Frequency Tuning Word 4[15:8]								0x00
	7:0	Frequency Tuning Word 4[7:0]								0x00
RAM Profile 4 (0x12)	63:56	Open								0x00
	55:48	RAM Profile 4 address step rate[15:8]								0x00
	47:40	RAM Profile 4 address step rate[7:0]								0x00
	39:32	RAM Profile 4 waveform end address[9:2]								0x00
	31:24	RAM Profile 4 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 4 waveform start address[9:2]								0x00
	15:8	RAM Profile 4 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 4 mode control[2:0]			0x00
Single Tone Profile 5 (0x13)	63:56	Open		Amplitude Scale Factor 5[13:8]						0x00
	55:48	Amplitude Scale Factor 5[7:0]								0x00
	47:40	Phase Offset Word 5[15:8]								0x00
	39:32	Phase Offset Word 5[7:0]								0x00
	31:24	Frequency Tuning Word 5[31:24]								0x00
	23:16	Frequency Tuning Word 5[23:16]								0x00
	15:8	Frequency Tuning Word 5[15:8]								0x00
	7:0	Frequency Tuning Word 5[7:0]								0x00

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value[1] (Hex)
RAM Profile 5 (0x13)	63:56	Open								0x00
	55:48	RAM Profile 5 address step rate[15:8]								0x00
	47:40	RAM Profile 5 address step rate[7:0]								0x00
	39:32	RAM Profile 5 waveform end address[9:2]								0x00
	31:24	RAM Profile 5 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 5 waveform start address[9:2]								0x00
	15:8	RAM Profile 5 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 5 mode control[2:0]			0x00
Single Tone Profile 6 (0x14)	63:56	Open		Amplitude Scale Factor 6[13:8]						0x00
	55:48	Amplitude Scale Factor 6[7:0]								0x00
	47:40	Phase Offset Word 6[15:8]								0x00
	39:32	Phase Offset Word 6[7:0]								0x00
	31:24	Frequency Tuning Word 6[31:24]								0x00
	23:16	Frequency Tuning Word 6[23:16]								0x00
	15:8	Frequency Tuning Word 6[15:8]								0x00
	7:0	Frequency Tuning Word 6[7:0]								0x00
RAM Profile 6 (0x14)	63:56	Open								0x00
	55:48	RAM Profile 6 address step rate[15:8]								0x00
	47:40	RAM Profile 6 address step rate[7:0]								0x00
	39:32	RAM Profile 6 waveform end address[9:2]								0x00
	31:24	RAM Profile 6 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 6 waveform start address[9:2]								0x00
	15:8	AM Profile 6 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 6 mode control[2:0]			0x00
Single Tone Profile 7 (0x15)	63:56	Open		Amplitude Scale Factor 7[13:8]						0x00
	55:48	Amplitude Scale Factor 7[7:0]								0x00
	47:40	Phase Offset Word 7[15:8]								0x00
	39:32	Phase Offset Word 7[7:0]								0x00
	31:24	Frequency Tuning Word 7[31:24]								0x00
	23:16	Frequency Tuning Word 7[23:16]								0x00
	15:8	Frequency Tuning Word 7[15:8]								0x00
	7:0	Frequency Tuning Word 7[7:0]								0x00
RAM Profile 7 (0x15)	63:56	Open								0x00
	55:48	RAM Profile 7 address step rate[15:8]								0x00
	47:40	RAM Profile 7 address step rate[7:0]								0x00
	39:32	RAM Profile 7 waveform end address[9:2]								0x00
	31:24	RAM Profile 7 waveform end address[1:0]		Open						0x00
	23:16	RAM Profile 7 waveform start address[9:2]								0x00
	15:8	RAM Profile 7 waveform start address[1:0]		Open						0x00
	7:0	Open		No-dwell high	Open	Zero-crossing	RAM Profile 7 mode control[2:0]			0x00
RAM (0x16)	31:0	RAM word[31:0]								0x00

[1] N/A = not applicable.

REGISTER BIT DESCRIPTIONS

The serial I/O port registers span an address range of 0 to 23 (0x00 to 0x16 in hexadecimal notation). This represents a total of 24 registers. However, two of these registers are unused, yielding a total of 22 available registers. The unused registers are Register 5 and Register 6 (0x05 and 0x06, respectively).

The number of bytes assigned to the registers varies. That is, the registers are not of uniform depth; each contains the number of bytes necessary for its particular function. Additionally, the registers are assigned names according to their functionality. In some cases, a register is given a mnemonic descriptor. For example, the register at Serial Address 0x00 is named Control Function Register 1 and is assigned the mnemonic CFR1.

The following section provides a detailed description of each bit in the MCDS9910 register map.
For cases in which a group of bits serves a specific function, the entire group is considered a
binary word and described in aggregate.

This section is organized in sequential order of the serial addresses of the registers. Each subheading includes the register name and optional register mnemonic (in parentheses). Also given is the serial address in hexadecimal format and the number of bytes assigned to the register.

Following each subheading is a table containing the individual bit descriptions for that particular register. The location of the bit(s) in the register is indicated by a single number or a pair of numbers separated by a colon; that is, a pair of numbers (A:B) indicates a range of bits from the most significant (A) to the least significant (B). For example, 5:2 implies Bit Position 5 down to Bit Position 2, inclusive, with Bit 0 identifying the LSB of the register.

Unless otherwise stated, programmed bits are not transferred to their internal destinations until the assertion of the I/O_UPDATE pin or a profile change.

Control Function Register 1 (CFR1)—Address 0x00

Four bytes are assigned to this register.

Table 5. Bit Description for CFR1

Bit(s)	Mnemonic	Description
31	RAM enable	0 = disables RAM functionality (default). 1 = enables RAM functionality (required for both load/retrieve and playback operation).
30:29	RAM playback destination	default is 00b.
28:24	Open	
23	Manual OSK external control	Ineffective unless CFR1[9:8] = 10b. 0 = OSK pin inoperative (default). 1 = OSK pin enabled for manual OSK control (see Output Shift Keying (OSK) section for details).
22	Inverse sinc filter enable	0 = inverse sinc filter bypassed (default). 1 = inverse sinc filter active.
21	Open	
20:17	Internal profile control	Ineffective unless CFR1[31] = 1. These bits are effective without the need for an I/O update. . Default is 0000b.
16	Select DDS sine output	0 = cosine output of the DDS is selected (default). 1 = sine output of the DDS is selected.
15	Load LRR @ I/O update	Ineffective unless CFR2[19] = 1. 0 = normal operation of the digital ramp timer (default). 1 = digital ramp timer loaded any time I/O_UPDATE is asserted or a PROFILE[2:0] change occurs.
14	Autoclear digital ramp accumulator	0 = normal operation of the DRG accumulator (default). 1 = the ramp accumulator is reset for one cycle of the DDS clock after which the accumulator automatically resumes normal operation. As long as this bit remains set, the ramp accumulator is momentarily reset each time an I/O_UPDATE is asserted or a PROFILE[2:0] change occurs. This bit is synchronized with either an I/O _UPDATE or a PROFILE[2:0] change and the next rising edge of SYNC_CLK.
13	Autoclear phase accumulator	0 = normal operation of the DDS phase accumulator (default). 1 = synchronously resets the DDS phase accumulator anytime I/O_UPDATE is asserted or a profile change occurs.

Bit(s)	Mnemonic	Description
12	Clear digital ramp accumulator	0 = normal operation of the DRG accumulator (default). 1 = asynchronous, static reset of the DRG accumulator. The ramp accumulator remains reset as long as this bit remains set. This bit is synchronized with either an I/O_UPDATE or a PROFILE[2:0] change and the next rising edge of SYNC_CLK.
11	Clear phase accumulator	0 = normal operation of the DDS phase accumulator (default). 1 = asynchronous, static reset of the DDS phase accumulator.
10	Load ARR @ I/O update	Ineffective unless CFR1[9:8] = 11b. 0 = normal operation of the OSK amplitude ramp rate timer (default). 1 = OSK amplitude ramp rate timer reloaded anytime I/O_UPDATE is asserted or a PROFILE[2:0] change occurs.
9	OSK enable	The output shift keying enable bit. 0 = OSK disabled (default). 1 = OSK enabled.
8	Select auto OSK	Ineffective unless CFR1[9] = 1. 0 = manual OSK enabled (default). 1 = automatic OSK enabled.
7	Digital power-down	This bit is effective without the need for an I/O update. 0 = clock signals to the digital core are active (default). 1 = clock signals to the digital core are disabled.
6	DAC power-down	0 = DAC clock signals and bias circuits are active (default). 1 = DAC clock signals and bias circuits are disabled.
5	REFCLK input power-down	This bit is effective without the need for an I/O update. 0 = REFCLK input circuits and PLL are active (default). 1 = REFCLK input circuits and PLL are disabled.
4	Auxiliary DAC power-down	0 = auxiliary DAC clock signals and bias circuits are active (default). 1 = auxiliary DAC clock signals and bias circuits are disabled.
3	External power-down control	0 = assertion of the EXT_PWR_DWN pin affects full power-down (default). 1 = assertion of the EXT_PWR_DWN pin affects fast recovery power-down.
2	Open	
1	SDIO input only	0 = configures the SDIO pin for bidirectional operation; 2-wire serial programming mode (default). 1 = configures the serial data I/O pin (SDIO) as an input only pin; 3-wire serial programming mode.
0	LSB first	0 = configures the serial I/O port for MSB-first format (default). 1 = configures the serial I/O port for LSB-first format.

Control Function Register 2 (CFR2)—Address 0x01

Four bytes are assigned to this register.

Table 6. Bit Descriptions for CFR2

Bit(s)	Mnemonic	Description
31:25	Open	
24	Enable amplitude scale from single tone profiles	Ineffective if CFR2[19] = 1 or CFR1[31] = 1 or CFR1[9] = 1. 0 = the amplitude scaler is bypassed and shut down for power conservation (default). 1 = the amplitude is scaled by the ASF from the active profile.
23	Internal I/O update active	This bit is effective without the need for an I/O update. 0 = serial I/O programming is synchronized with the external assertion of the I/O_UPDATE pin, which is configured as an input pin (default). 1 = serial I/O programming is synchronized with an internally generated I/O update signal (the internally generated signal appears at the I/O_UPDATE pin, which is configured as an output pin).
22	SYNC_CLK enable	0 = the SYNC_CLK pin is disabled; static Logic 0 output. 1 = the SYNC_CLK pin generates a clock signal at ¼ f_{SYSCLK}; used for synchronization of the serial I/O port (default).
21:20	Digital ramp destination	Default is 00b. See the Digital Ramp Generator (DRG) section for details.
19	Digital ramp enable	0 = disables digital ramp generator functionality (default). 1 = enables digital ramp generator functionality.
18	Digital ramp no-dwell high	See the Digital Ramp Generator (DRG) section for details. 0 = disables no-dwell high functionality (default). 1 = enables no-dwell high functionality.
17	Digital ramp no-dwell low	See the Digital Ramp Generator (DRG) section for details. 0 = disables no-dwell low functionality (default). 1 = enables no-dwell low functionality.
16	Read effective FTW	0 = a serial I/O port read operation of the FTW register reports the contents of the FTW register (default). 1 = a serial I/O port read operation of the FTW register reports the actual 32-bit word appearing at the input to the DDS phase accumulator.
15:14	I/O update rate control	Ineffective unless CFR2[23] = 1. Sets the prescale ratio of the divider that clocks the auto I/O update timer as follows: 00 = divide-by-1 (default). 01 = divide-by-2. 10 = divide-by-4. 11 = divide-by-8.
13:12	Open	
11	PDCLK enable	0 = the PDCLK pin is disabled and forced to a static Logic 0 state; the internal clock signal continues to operate and provide timing to the data assembler. 1 = the internal PDCLK signal appears at the PDCLK pin (default).
10	PDCLK invert	0 = normal PDCLK polarity; Q-data associated with Logic 1, I-data with Logic 0 (default). 1 = inverted PDCLK polarity.
9	TxEnable invert	0 = no inversion. 1 = inversion.
8	Open	
7	Matched latency enable	0 = simultaneous application of amplitude, phase, and frequency changes to the DDS arrive at the output in the order listed (default). 1 = simultaneous application of amplitude, phase, and frequency changes to the DDS arrive at the output simultaneously.

Bit(s)	Mnemonic	Description
6	Data assembler hold last value	Ineffective unless CFR2[4] = 1. 0 = the data assembler of the parallel data port internally forces zeros on the data path and ignores the signals on the D[15:0] and F[1:0] pins while the TxENABLE pin is Logic 0 (default). This implies that the destination of the data at the parallel data port is amplitude when TxENABLE is Logic 0. 1 = the data assembler of the parallel data port internally forces the last value received on the D[15:0] and F[1:0] pins while the TxENABLE pin is Logic 1.
5	Sync timing validation disable	0 = enables the SYNC_SMP_ERR pin to indicate (active high) detection of a synchronization pulse sampling error. 1 = the SYNC_SMP_ERR pin is forced to a static Logic 0 condition (default).
4	Parallel data port enable	See the Parallel Data Port Modulation Mode section for more details. 0 = disables parallel data port modulation functionality (default). 1 = enables parallel data port modulation functionality.
3:0	FM gain	See the Parallel Data Port Modulation Mode section for more details. Default is 0000b.

Control Function Register 3 (CFR3)—Address 0x02

Four bytes are assigned to this register.

Table 7. Bit Descriptions for CFR3

Bit(s)	Mnemonic	Description
31:30	Open	
29:28	DRV0	Controls the REFCLK_OUT pin (see Table 7 for details); default is 01b.
27	Open	
26:24	VCO SEL	Selects the frequency band of the REFCLK PLL VCO (see Table 8 for details); default is 111b.
23:22	Open	
21:19	I_{CP}	Selects the charge pump current in the REFCLK PLL (see Table 9 for details); default is 111b.
18:16	Open	
15	REFCLK input divider bypass	0 = input divider is selected (default). 1 = input divider is bypassed.
14	REFCLK input divider ResetB	0 = input divider is reset. 1 = input divider operates normally (default).
13:11	Open	
10	PFD reset	0 = normal operation (default). 1 = phase detector disabled.
9	Open	
8	PLL enable	0 = REFCLK PLL bypassed (default). 1 = REFCLK PLL enabled.
7:1	N	This 7-bit number is the divide modulus of the REFCLK PLL feedback divider; default is 0000000b.
0	Open	

Auxiliary DAC Control Register—Address 0x03

Four bytes are assigned to this register.

Table 8. Bit Descriptions for DAC Control Register

Bit(s)	Mnemonic	Description
31:8	Open	
7:0	FSC	This 8-bit number controls the full-scale output current of the main DAC (see the Auxiliary DAC section); default is 0x7F.

I/O Update Rate Register—Address 0x04

Four bytes are assigned to this register. This register is effective without the need for an I/O update.

Table 9. Bit Descriptions for I/O Update Rate Register

Bit(s)	Mnemonic	Description
31:0	I/O update rate	Ineffective unless CFR2[23] = 1. This 32-bit number controls the automatic I/O update rate (see the Automatic I/O Update section for details); default is 0xFFFFFFFF.

Frequency Tuning Word Register (FTW)—Address 0x07

Four bytes are assigned to this register.

Table 10. Bit Descriptions for FTW Register

Bit(s)	Mnemonic	Description
31:0	Frequency tuning word	32-bit frequency tuning word.

Phase Offset Word Register (POW)—Address 0x08

Two bytes are assigned to this register.

Table 11. Bit Descriptions for POW Register

Bit(s)	Mnemonic	Description
15:0	Phase offset word	16-bit phase offset word.

Amplitude Scale Factor Register (ASF)—Address 0x09

Four bytes are assigned to this register.

Table 12. Bit Descriptions for ASF Register

Bit(s)	Mnemonic	Description
31:16	Amplitude ramp rate	16-bit amplitude ramp rate value. Effective only if CFR1[9:8] = 11b; see the Output Shift Keying (OSK) section for details.
15:2	Amplitude scale factor	14-bit amplitude scale factor.
1:0	Amplitude step size	Effective only if CFR1[9:8] = 11b; see the Output Shift Keying (OSK) section for details.

Multichip Sync Register—Address 0x0A

Four bytes are assigned to this register.

Table 13. Multichip Sync Register

Bit(s)	Mnemonic	Description
31:28	Sync validation delay	This 4-bit number sets the timing skew (in ~75ps increments) between SYSCLK and the delayed SYNC_INx signal for the sync validation block in the sync receiver. Default is 0000b.
27	Sync receiver enable	0 = synchronization clock receiver disabled (default). 1 = synchronization clock receiver enabled.
26	Sync generator enable	0 = synchronization clock generator disabled (default). 1 = synchronization clock generator enabled.
25	Sync generator polarity	0 = synchronization clock generator coincident with the rising edge of SYSCLK (default). 1 = synchronization clock generator coincident with the falling edge of SYSCLK.
24	Open	
23:18	Sync state preset value	This 6-bit number is the state that the internal clock generator assumes when it receives a sync pulse. Default is 000000b.
17:16	Open	
15:11	Output sync generator delay	This 5-bit number sets the output delay (in ~75 ps increments) of the sync generator. Default is 00000b.
10:8	Open	
7:3	Input sync receiver delay	This 5-bit number sets the input delay (in ~75 ps increments) of the sync receiver. Default is 00000b.
2:0	Open	

Digital Ramp Limit Register—Address 0x0B

Eight bytes are assigned to this register. This register is only effective if CFR2[19] = 1. See the Digital Ramp Generator (DRG) section for details.

Table 14. Bit Descriptions for Digital Ramp Limit Register

Bit(s)	Mnemonic	Description
63:32	Digital ramp upper limit	32-bit digital ramp upper limit value.
31:0	Digital ramp lower limit	32-bit digital ramp lower limit value.

Digital Ramp Step Size Register—Address 0x0C

Eight bytes are assigned to this register. This register is only effective if CFR2[19] = 1. See the Digital Ramp Generator (DRG) section for details.

Table 15. Bit Descriptions for Digital Ramp Step Size Register

Bit(s)	Mnemonic	Description
63:32	Digital ramp decrement step size	32-bit digital ramp decrement step size value.
31:0	Digital ramp increment step size	32-bit digital ramp increment step size value.

Digital Ramp Rate Register—Address 0x0D

Four bytes are assigned to this register. This register is only effective if CFR2[19] = 1. See the Digital Ramp Generator (DRG) section for details.

Table 16. Bit Descriptions for Digital Ramp Rate Register

Bit(s)	Mnemonic	Description
31:16	Digital ramp negative slope rate	16-bit digital ramp negative slope value that defines the time interval between decrement values.
15:0	Digital ramp positive slope rate	16-bit digital ramp positive slope value that defines the time interval between increment values.

Profile Registers

There are eight consecutive serial I/O addresses (Address 0x0E to Address 0x015) dedicated to device profiles. All eight profile registers are either single tone profiles or RAM profiles. RAM profiles are in effect when CFR1[31] = 1. Single tone profiles are in effect when CFR1[31] = 0, CFR2[19] = 0, and CFR2[4] = 0.

In normal operation, the active profile register is selected using the external PROFILE[2:0] pins. However, in the specific case when CFR1[31] = 1 and CFR1[20:17] ≠ 0000b, the active profile is selected automatically (see the RAM Ramp-Up Internal Profile Control Mode section).

Profile 0 to Profile 7, Single Tone Registers—Address 0x0E to Address 0x15

Eight bytes are assigned to each register.

Table 17. Bit Descriptions for Profile 0 to Profile 7 Single Tone Register

Bit(s)	Mnemonic	Description
63:62	Open	
61:48	Amplitude scale factor	This 14-bit number controls the DDS output amplitude.
47:32	Phase offset word	This 16-bit number controls the DDS phase offset.
31:0	Frequency tuning word	This 32-bit number controls the DDS frequency.

RAM Profile 0 to RAM Profile 7, Control Registers—Address 0x0E to Address 0x15

Eight bytes are assigned to each register.

Table 18. Bit Descriptions for Profile 0 to Profile 7 RAM Register

Bit(s)	Mnemonic	Description
63:56	Open	
55:40	Address step rate	16-bit address step rate value.
39:30	Waveform end address	10-bit waveform end address.
29:24	Open	
23:14	Waveform start address	10-bit waveform start address.
13:6	Open	
5	No-dwell high	Effective only when the RAM mode is in ramp-up. 0 = when the RAM state machine reaches the end address, it halts. 1 = when the RAM state machines reaches the end address, it jumps to the start address and halts.
4	Open	
3	Zero-crossing	Effective only when in RAM mode, direct switch. 0 = zero-crossing function disabled. 1 = zero-crossing function enabled.
2:0	RAM mode control	See Table 13 for details.

RAM Register—Address 0x16

Four bytes are assigned to the RAM register.

Table 19. Bit Descriptions for RAM Register

Bit(s)	Mnemonic	Description
31:0	RAM word	The start and end addresses in the RAM Profile 0 to RAM Profile 7 control registers define the number of 32-bit words (1 minimum, 1024 maximum) to be written to the RAM register.

OUTLINE DIMENSIONS

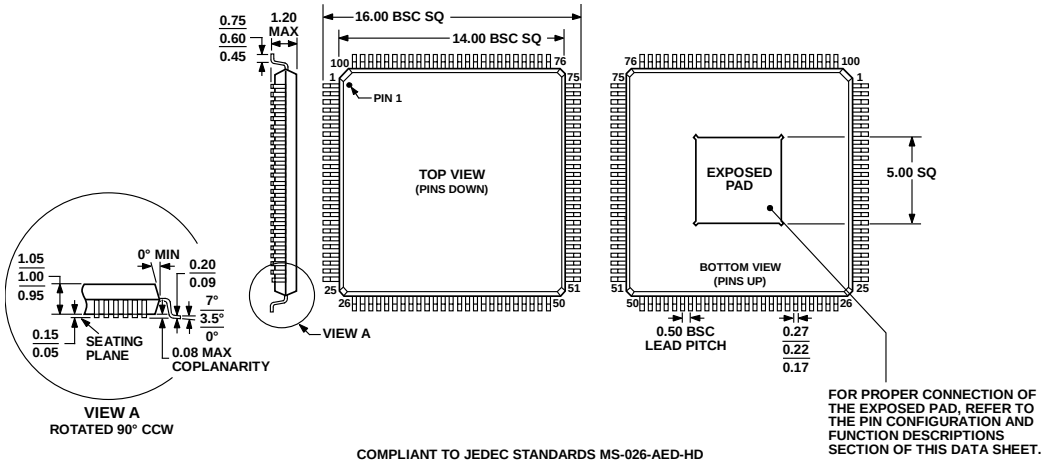


Figure 7. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9910BSVZ	–40°C to +85°C	100-Lead TQFP	Tray/900

[1] Z = RoHS Compliant Part.

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