米米克微电子

1 GSPS Quadrature Digital Upconverter with 18-Bit I/Q Data Path and 14-Bit DAC

Data Sheet

MCD9957

FEATURES

- 1 GSPS internal clock speed (up to 400 MHz analog output)
- Integrated 1 GSPS 14-bit DAC
- 250 MSPS input data rate
- Phase noise ≤ −124 dBc/Hz (400 MHz carrier at 1 kHz offset)
- Excellent dynamic performance >80 dB narrow-band SFDR
- 8 programmable profiles for shift keying
- Sin(x)/(x) correction (inverse sinc filter)
- Reference clock multiplier
- Internal oscillator for a single crystal operation
- Software and hardware controlled power-down
- Integrated RAM
- Phase modulation capability
- Multichip synchronization
- Easy interface to Blackfin SPORT
- Interpolation factors from 4× to 252×
- Gain control DAC
- Internal divider allows references up to 2 GHz
- 1.8 V and 3.3 V power supplies
- 100-lead TQFP_EP package

APPLICATIONS

- HFC data, telephony, and video modems
- Wireless base station transmissions
- Broadband communications transmissions
- Internet telephony

GENERAL DESCRIPTION

The MCD9957 functions as a universal I/Q modulator and agile upconverter for communications systems where cost, size, power consumption, and dynamic performance are critical. The MCD9957 integrates a high speed, direct digital synthesizer (DDS), a high performance, high speed, 14-bit digital-to-analog converter (DAC), clock multiplier circuitry, digital filters, and other DSP functions onto a single chip. It provides baseband upconversion for data transmission in a wired or wireless communications system.

Unlike its predecessors, it supports a 16-bit serial input mode for I/Q baseband data. The device can alternatively be programmed to operate either as a single tone, sinusoidal source or as an interpolating DAC.

The reference clock input circuitry includes a crystal oscillator, a high speed, divide-by-two input, and a low noise PLL for multiplication of the reference clock frequency.

FUNCTIONAL BLOCK DIAGRAM

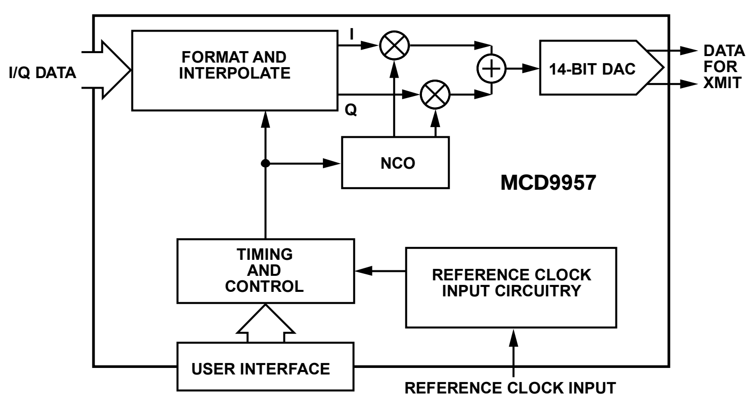


Figure 1.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

AVDD (1.8V) and DVDD (1.8V) = 1.8 V ± 5%, AVDD (3.3V) = 3.3 V ± 5%, DVDD_I/O (3.3V) = 3.3 V ± 5%, T = 25°C, R_{SET} = 10 kΩ, I_{OUT} = 20 mA, external reference clock frequency = 1000 MHz with REFCLK multiplier disabled, unless otherwise noted.

Table 1.

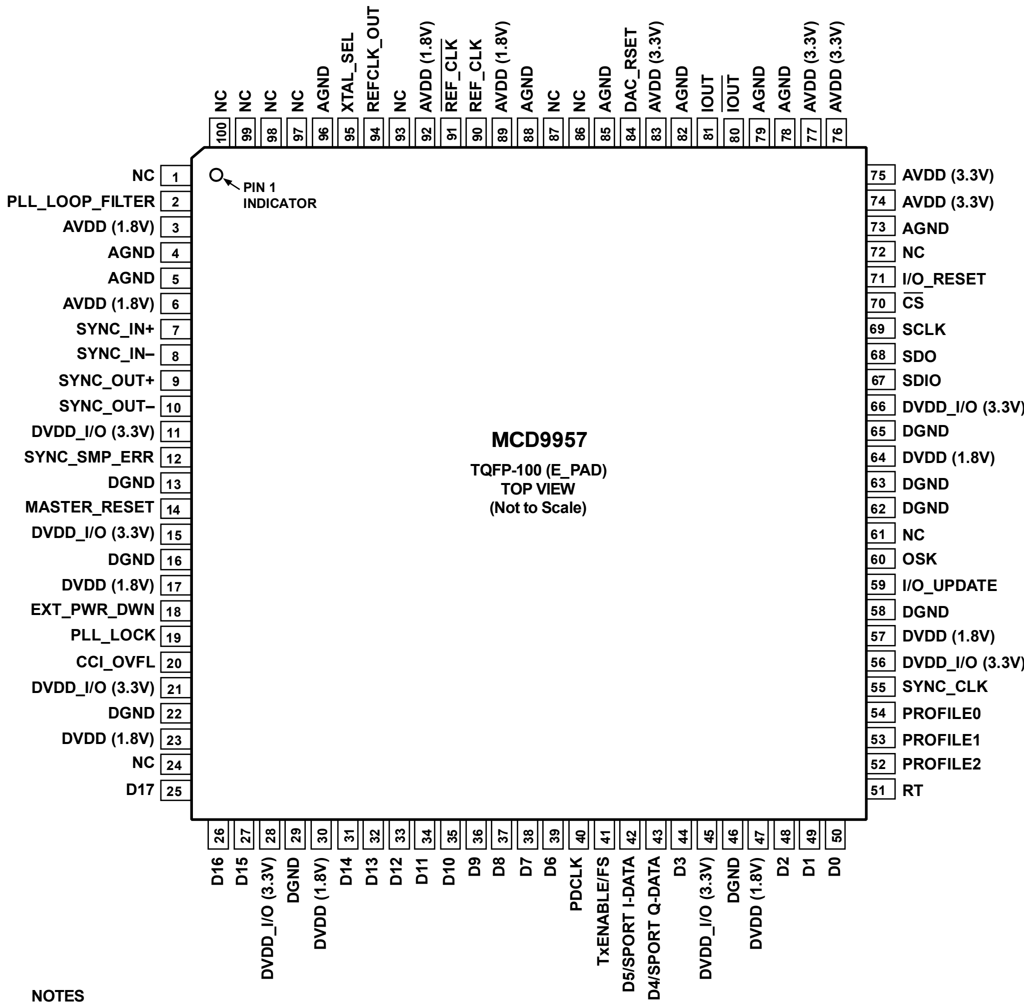
Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REF_CLK INPUT CHARACTERISTICS					
Frequency Range					
REFCLK Multiplier	Disabled	60		1000	MHz
	Enabled	3.2		60	MHz
Maximum REFCLK Input Divider Frequency	Full temperature range	1500	1900		MHz
Minimum REFCLK Input Divider Frequency	Full temperature range		25	35	MHz
External Crystal			25		MHz
Input Capacitance			3.2		pF
Input Impedance (Differential)			2.9		kΩ
Input Impedance (Single-Ended)			1.45		kΩ
Duty Cycle	REFCLK multiplier disabled	45		55	%
	REFCLK multiplier enabled	40		60	%
REF_CLK Input Level	Single-ended	50		1000	mV p-p
	Differential	100		2000	mV p-p
REFCLK MULTIPLIER VCO GAIN CHARACTERISTICS					
VCO Gain (K_V) at Center Frequency	VCO0 range setting		432		MHz/V
	VCO1 range setting		505		MHz/V
	VCO2 range setting		560		MHz/V
	VCO3 range setting		754		MHz/V
	VCO4 range setting		785		MHz/V
	VCO5 range setting[2]		853		MHz/V
REFCLK_OUT CHARACTERISTICS					
Maximum Capacitive Load			20		pF
Maximum Frequency			25		MHz
DAC OUTPUT CHARACTERISTICS					
Full-Scale Output Current		8.5	20	31.5	mA
Gain Error		−10		+10	%FS
Output Offset				3.4	µA
Differential Nonlinearity			0.9		LSB
Integral Nonlinearity			1.7		LSB
Output Capacitance			4.5		pF
Residual Phase Noise	At 1 kHz offset, 20 MHz A_{OUT}				
REFCLK Multiplier	Disabled		−150		dBc/Hz
	Enabled at 20×		−141		dBc/Hz
	Enabled at 100×		−139		dBc/Hz
AC Voltage Compliance Range		−0.5		+0.5	V
SPURIOUS-FREE DYNAMIC RANGE (SFDR SINGLE TONE)					
f_{OUT} = 20.1 MHz			−69		dBc
f_{OUT} = 98.6 MHz			−68		dBc
f_{OUT} = 201.1 MHz			−64		dBc
f_{OUT} = 397.8 MHz			−55		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE SPECTRAL DENSITY (NSD)					
Single Tone					
f_{OUT} = 20.1 MHz			−166		dBm/Hz
f_{OUT} = 98.6 MHz			−160		dBm/Hz
f_{OUT} = 201.1 MHz			−155		dBm/Hz
f_{OUT} = 397.8 MHz			−150		dBm/Hz
TWO-TONE INTERMODULATION DISTORTION (IMD)	I/Q rate = 62.2 MSPS; 16× interpolation				
f_{OUT} = 25 MHz			−81		dBc
f_{OUT} = 50 MHz			−76		dBc
f_{OUT} = 100 MHz			−71		dBc
MODULATOR CHARACTERISTICS					
Input Data					
Error Vector Magnitude	2.5 Msymbols/s, QPSK, 4× oversampled		0.58		%
	270.8333 ksymbols/s, GMSK, 32× oversampled		0.79		%
	2.5 Msymbols/s, 256-QAM, 4× oversampled		0.38		%
WCDMA—FDD (TM1), 3.84 MHz Bandwidth, 5 MHz Channel Spacing					
Adjacent Channel Leakage Ratio (ACLR)	IF = 143.88 MHz		−76		dBc
Carrier Feedthrough			−77		dBc
SERIAL PORT TIMING CHARACTERISTICS					
Maximum SCLK Frequency			70		Mbps
Minimum SCLK Pulse Width	Low	4.5			ns
	High	4.5			ns
Maximum SCLK Rise/Fall Time			2.2		ns
Minimum Data Setup Time to SCLK		6			ns
Minimum Data Hold Time to SCLK		0			ns
Maximum Data Valid Time in Read Mode				11	ns
I/O_UPDATE/PROFILE2 to PROFILE 0/RT TIMING CHARACTERISTICS					
Minimum Pulse Width	High	1			SYNC_CLK cycle
Minimum Setup Time to SYNC_CLK		1.78			ns
Minimum Hold Time to SYNC_CLK		0			ns
I/Q INPUT TIMING CHARACTERISTICS					
Maximum PDCLK Frequency			250		MHz
Minimum I/Q Data Setup Time to PDCLK		1.70			ns
Minimum I/Q Data Hold Time to PDCLK		0			ns
Minimum TxENABLE Setup Time to PDCLK		1.70			ns
Minimum TxENABLE Hold Time to PDCLK		0			ns
MISCELLANEOUS TIMING CHARACTERISTICS					
Wake-Up Time[3]			1		
Fast Recovery Mode			8		SYSCLK cycles[4]
Full Sleep Mode				153	µs
Minimum Reset Pulse Width High			5		SYSCLK cycles[4]
DATA LATENCY (PIPELINE DELAY)					
Data Latency Single Tone Mode					
Frequency, Phase and Amplitude-to-DAC output	Match delay enable		91		SYSCLK cycles[4]
Frequency, Phase-to-DAC Output	Match delay disabled		79		SYSCLK cycles[4]

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SYSCLK CYCLE					
Voltage					
Logic 1		2.0			V
Logic 0				0.8	V
Current					
Logic 1			93	123	µA
Logic 0			39	51	µA
Input Capacitance			2.3		pF
XTAL_SEL INPUT					
Logic 1 Voltage		1.25			V
Logic 0 Voltage				0.6	V
Input Capacitance		2.3			pF
CMOS LOGIC OUTPUTS	1 mA load				
Voltage					
Logic 1		2.8			V
Logic 0				0.4	V
POWER SUPPLY CURRENT					
DVDD_I/O (3.3V) Pin Current Consumption	QDUC mode		18		mA
DVDD (1.8V) Pin Current Consumption	QDUC mode		615		mA
AVDD (3.3V) Pin Current Consumption	QDUC mode		29		mA
AVDD (1.8V) Pin Current Consumption	QDUC mode		109		mA
POWER CONSUMPTION					
Single Tone Mode			810		mW
Continuous Modulation	8× interpolation		1415	1820	mW
Inverse Sinc Filter Power Consumption			155	208	mW
Full Sleep Mode			15	30	mW

[1] The system clock is limited to 750 MHz maximum in BFI mode.
[2] The gain value for VCO range Setting 5 is measured at 1000 MHz.
[3] Wake-up time refers to the recovery from analog power-down modes. The longest time required is for the Reference Clock Multiplier PLL to relock to the reference.
[4] SYSCLK cycle refers to the actual clock frequency used on-chip by the DDS. If the reference clock multiplier is used to multiply the external reference clock frequency, the SYSCLK frequency is the external frequency multiplied by the reference clock multiplication factor. If the reference clock multiplier and divider are not used, the SYSCLK frequency is the same as the external reference clock frequency.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. EXPOSED PAD SHOULD BE SOLDERED TO GROUND.

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	Description
1, 24, 61, 72, 86, 87, 93, 97 to 100	NC		Not Connected. Allow the device pin to float.
2	PLL_LOOP_FILTER	I	PLL Loop Filter Compensation. See External PLL Loop Filter Components section.
3, 6, 89, 92	AVDD (1.8V)	I	Analog Core VDD. 1.8 V analog supplies.
74 to 77, 83	AVDD (3.3V)	I	Analog DAC VDD. 3.3 V analog supplies.
17, 23, 30, 47, 57, 64	DVDD (1.8V)	I	Digital Core VDD. 1.8 V digital supplies.
11, 15, 21, 28, 45, 56, 66	DVDD_I/O (3.3V)	I	Digital Input/Output VDD. 3.3 V digital supplies.
4, 5, 73, 78, 79, 82, 85, 88, 96	AGND	I	Analog Ground.
13, 16, 22, 29, 46, 58, 62, 63, 65	DGND	I	Digital Ground.
7	SYNC_IN+	I	Synchronization Signal, Digital Input (Rising Edge Active). Synchronization signal from external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section.
8	SYNC_IN−	I	Synchronization Signal, Digital Input (Falling Edge Active). Synchronization signal from external master to synchronize internal subclocks. See the Synchronization of Multiple Devices section.
9	SYNC_OUT+	O	Synchronization Signal, Digital Output (Rising Edge Active). Synchronization signal from internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section.
10	SYNC_OUT−	O	Synchronization Signal, Digital Output (Falling Edge Active). Synchronization signal from internal device subclocks to synchronize external slave devices. See the Synchronization of Multiple Devices section.
12	SYNC_SMP_ERR	O	Synchronization Sample Error, Digital Output (Active High). A high on this pin indicates that the MCD9957 did not receive a valid sync signal on SYNC_IN+/SYNC_IN −. See the Synchronization of Multiple Devices section.
14	MASTER_RESET	I	Master Reset, Digital Input (Active High). This pin clears all memory elements and sets registers to default values.
18	EXT_PWR_DWN	I	External Power-Down, Digital Input (Active High). A high level on this pin initiates the currently programmed power-down mode. See the Power-Down Control section for further details. If unused, tie to ground.
19	PLL_LOCK	O	PLL Lock, Digital Output (Active High). A high on this pin indicates that the clock multiplier PLL has acquired lock to the reference clock input.
20	CCI_OVFL	O	CCI Overflow Digital Output, Active High. A high on this pin indicates a CCI filter overflow. This pin remains high until the CCI overflow condition is cleared.
25 to 27, 31 to 39, 42 to 44, 48 to 50	D[17:0]	I/O	Parallel Data Input Bus (Active High). These pins provide the interleaved, 18-bit, digital, I and Q vectors for the modulator to upconvert. Also used for a GPIO port in Blackfin interface mode.
42	SPORT I-DATA	I	I-Data Serial Input. In Blackfin interface mode, this pin serves as the I-data serial input.
43	SPORT Q-DATA	I	Q-Data Serial Input. In Blackfin interface mode, this pin serves as the Q-data serial input.
40	PDCLK	O	Parallel Data Clock, Digital Output (Clock). See the Signal Processing section for details.
41	TxENABLE/FS	I	Transmit Enable, Digital Input (Active High). See the Signal Processing section for details. In Blackfin interface mode, this pin serves as the FS input to receive the RFS output signal from the Blackfin.
51	RT	I	RAM Trigger, Digital Input (Active High). This pin provides control for the RAM amplitude scaling function. When this function is engaged, a high sweeps the amplitude from the beginning RAM address to the end. A low sweeps the amplitude from the end RAM address to the beginning. If unused, connect to ground or supply.
52 to 54	PROFILE2, PROFILE1, PROFILE0	I	Profile Select Pins, Digital Inputs (Active High). These pins select one of eight phase/frequency profiles for the DDS core (single tone or carrier tone). Changing the state of one of these pins transfers the current contents of all I/O buffers to the corresponding registers. Set up state changes to the SYNC_CLK pin.
55	SYNC_CLK	O	Output System Clock/4, Digital Output (Clock). Set up the I/O_UPDATE and PROFILE2/PROFILE1/PROFILE0 pins to the rising edge of this signal.

Pin No.	Mnemonic	I/O[1]	Description
59	I/O_UPDATE	I/O	Input/Output Update; Digital Input Or Output (Active High), Depending on the Internal I/O Update Active Bit. A high on this pin indicates a transfer of the contents of the I/O buffers to the corresponding internal registers.
60	OSK	I	Output Shift Keying, Digital Input (Active High). When using OSK (manual or automatic), this pin controls the OSK function. See the Output Shift Keying (OSK) section of the data sheet for details. When not using OSK, tie this pin high.
67	SDIO	I/O	Serial Data Input/Output, Digital Input/Output (Active High). This pin can be either unidirectional or bidirectional (default), depending on configuration settings. In bidirectional serial port mode, this pin acts as the serial data input and output. In unidirectional, it is an input only.
68	SDO	O	Serial Data Output, Digital Output (Active High). This pin is only active in unidirectional serial data mode. In this mode, it functions as the output. In bidirectional mode, this pin is not operational and must be left floating.
69	SCLK	I	Serial Data Clock. Digital clock (rising edge on write, falling edge on read). This pin provides the serial data clock for the control data path. Write operations to the MCD9957 use the rising edge. Readback operations from the MCD9957 use the falling edge.
70	$\overline{\text{CS}}$	I	Chip Select, Digital Input (Active Low). Bringing this pin low enables the MCD9957 to detect serial clock rising/falling edges. Bringing this pin high causes the MCD9957 to ignore input on the serial data pins.
71	I/O_RESET	I	Input/Output Reset. Digital input (active high). This pin can be used when a serial I/O communication cycle fails (see the I/O_RESET—Input/Output Reset section for details). When not used, connect this pin to ground.
80	$\overline{\text{IOUT}}$	O	Open-Source DAC Complementary Output Source. Analog output, current mode. Connect through 50 Ω to AGND.
81	IOUT	O	Open-Source DAC Output Source. Analog output, current mode. Connect through 50 Ω to AGND.
84	DAC_RSET	O	Analog Reference Pin. This pin programs the DAC output full-scale reference current. Attach a 10 kΩ resistor to AGND.
90	REF_CLK	I	Reference Clock Input. Analog input. See the REFCLK Overview section for more details.
91	$\overline{\text{REF\_CLK}}$	I	Complementary Reference Clock Input. Analog input. See the REFCLK Overview section for more details.
94	REFCLK_OUT	O	Reference Clock Output. Analog output. See the REFCLK Overview section for more details.
95	XTAL_SEL	I	Crystal Select (1.8 V Logic). Analog input (active high). Driving the XTAL_SEL pin high enables the internal oscillator to be used with a crystal resonator. If unused, connect it to AGND.
	EPAD		Exposed Pad (EPAD). The exposed pad should be soldered to ground.

[1] I is input, O is output, and I/O is for input/output.

SERIAL I/O TIMING DIAGRAMS

Figure 3 through Figure 6 provide basic examples of the tim-ing relationships between the various control signals of the serial I/O port.Most Most of the bits in the register map are not transferred to their internal destinations until assertion of an I/O update, which is not included in the timing diagrams that follow.

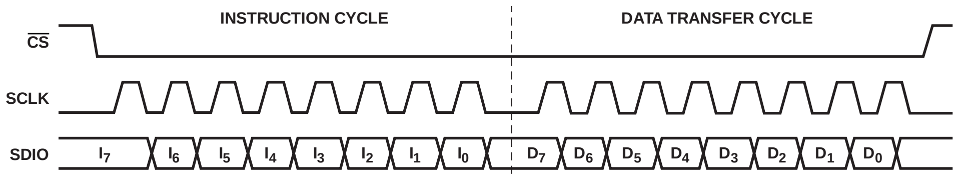


Figure 3 . Serial Port Write Timing—Clock Stall Low

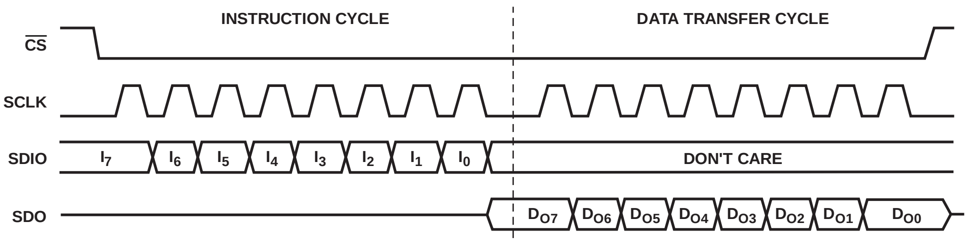


Figure 4 . 3-Wire Serial Port Read Timing—Clock Stall Low

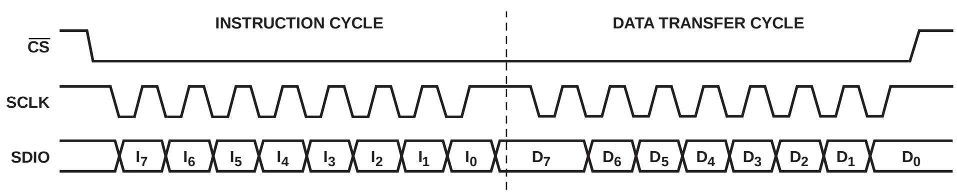


Figure 5 . Serial Port Write Timing—Clock Stall High

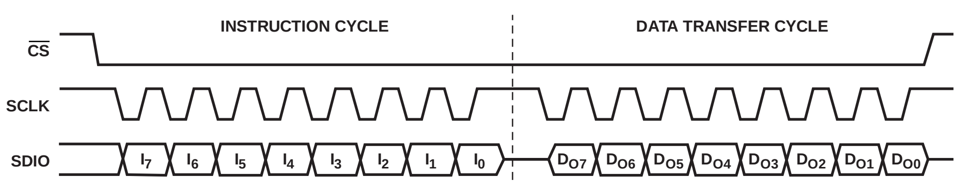


Figure 6. 2-Wire Serial Port Read Timing—Clock Stall High

REGISTER MAP AND BIT DESCRIPTIONS

REGISTER MAP

Note that the highest number found in the Bit Range column for each register in the following tables is the MSB and the lowest number is the LSB for that register.

Table 3. Control Registers

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
Control Function Register 1 CFR1 (0x00)	[31:24]	RAM Enable	Open		RAM Playback Destination	Open		Operating Mode		0x00
	[23:16]	Manual OSK External Control	Inverse Sinc Filter Enable	Clear CCI	Open				Select DDS Sine Output	0x00
	[15:8]	Open		Autoclear Phase Accumulator	Open	Clear Phase Accumulator	Load ARR at I/O Update	OSK Enable	Select Auto-OSK	0x00
	[7:0]	Digital Power-Down	DAC Power-Down	REFCLK Input Power-Down	Aux DAC Power-Down	External Power-Down Control	Auto Power-Down Enable	SDIO Input Only	LSB First	0x00
Control Function Register 2 CFR2 (0x01)	[31:24]	Blackfin Interface Mode Active	Blackfin Bit Order	Blackfin Early Frame Sync Enable	Open				Enable Profile Registers as ASF Source	0x00
	[23:16]	Internal I/O Update Active	SYNC_CLK Enable	Open					Read Effective FTW	0x40
	[15:8]	I/O Update Rate Control		PDCLK Rate Control	Data Format	PDCLK Enable	PDCLK Invert	TxENABLE Invert	Q-First Data Pairing	0x08
	[7:0]	Open	Data Assembler Hold Last Value	Sync Timing Validation Disable	Open					0x20
Control Function Register 3 CFR3 (0x02)	[31:24]	Open		DRV0[1:0]		Open	VCO SEL[2:0]			0x1F
	[23:16]	Open		I_{CP}[2:0]			Open			0x3F
	[15:8]	REFCLK Input Divider Bypass	REFCLK Input Divider ResetB	Open					PLL Enable	0x40
	[7:0]	N[6:0]							Open	0x00
Auxiliary DAC Control Register (0x03)	[31:24]	Open								0x00
	[23:16]	Open								0x00
	[15:8]	Open								0x7F
	[7:0]	FSC[7:0]								0x7F
I/O Update Rate Register (0x04)	[31:24]	I/O Update Rate[31:24]								0xFF
	[23:16]	I/O Update Rate[23:16]								0xFF
	[15:8]	I/O Update Rate[15:8]								0xFF
	[7:0]	I/O Update Rate[7:0]								0xFF

Table 4. RAM, ASF, Multichip Sync, and Profile 0 Registers

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
RAM Segment Register 0 (0x05)	[47:40]	RAM Address Step Rate 0[15:8]								
	[39:32]	RAM Address Step Rate 0[7:0]								
	[31:24]	RAM End Address 0[9:2]								
	[23:16]	RAM End Address 0[1:0]		Open						
	[15:8]	RAM Start Address 0[9:2]								
	[7:0]	RAM Start Address 0[1:0]		Open			RAM Playback Mode 0[2:0]			
RAM Segment Register 1 (0x06)	[47:40]	RAM Address Step Rate 1[15:8]								
	[39:32]	RAM Address Step Rate 1[7:0]								
	[31:24]	RAM End Address 1[9:2]								
	[23:16]	RAM End Address 1[1:0]		Open						
	[15:8]	RAM Start Address 1[9:2]								
	[7:0]	RAM Start Address 1[1:0]		Open			RAM Playback Mode 1[2:0]			
Amplitude Scale Factor (ASF) Register (0x09)	[31:24]	Amplitude Ramp Rate[15:8]								0x00
	[23:16]	Amplitude Ramp Rate[7:0]								0x00
	[15:8]	Amplitude Scale Factor]13:6]								0x00
	[7:0]	Amplitude Scale Factor[5:0]						Amplitude Step Size[1:0]		0x00
Multichip Sync Register (0x0A)	[31:24]	Sync Validation Delay[3:0]				Sync Receiver Enable	Sync Generator Enable	Sync Generator Polarity	Open	0x00
	[23:16]	Sync State Preset Value[5:0]						Open		0x00
	[15:8]	Sync Generator Delay[4:0]					Open			0x00
	[7:0]	Sync Receiver Delay[4:0]					Open			0x00
Profile 0 Register—Single Tone (0x0E)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 0 Register—QDUC (0x0E)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	N/A
	[55:48]	Output Scale Factor								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A

Table 5. Profile 1, Profile 2, and Profile 3 Registers

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
Profile 1 Register—Single Tone (0x0F)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 1 Register—QDUC (0x0F)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	N/A
	[55:48]	Output Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 2 Register—Single Tone (0x10)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 2 Register—QDUC (0x10)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	N/A
	[55:48]	Output Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 3 Register—Single Tone (0x11)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 3 Register—QDUC (0x11)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	N/A
	[55:48]	Output Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A

Table 6. Profile 4, Profile 5, and Profile 6 Registers

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
Profile 4 Register—Single Tone (0x12)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 4 Register—QDUC (0x12)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	N/A
	[55:48]	Output Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 5 Register—Single Tone (0x13)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 5 Register—QDUC (0x13)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	N/A
	[55:48]	Output Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 6 Register—Single Tone (0x14)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 6 Register—QDUC (0x14)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	N/A
	[55:48]	Output Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A

Table 7. Profile 7, RAM, GPIO Configuration, and GPIO Data Registers

Register Name (Serial Address)	Bit Range (Internal Address)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value
Profile 7 Register—Single Tone (0x15)	[63:56]	Open		Amplitude Scale Factor[13:8]						N/A
	[55:48]	Amplitude Scale Factor[7:0]								N/A
	[47:40]	Phase Offset Word[15:8]								N/A
	[39:32]	Phase Offset Word[7:0]								N/A
	[31:24]	Frequency Tuning Word[31:24]								N/A
	[23:16]	Frequency Tuning Word[23:16]								N/A
	[15:8]	Frequency Tuning Word[15:8]								N/A
	[7:0]	Frequency Tuning Word[7:0]								N/A
Profile 7 Register—QDUC (0x15)	[63:56]	CCI Interpolation Rate[7:2]						Spectral Invert	Inverse CCI Bypass	
	[55:48]	Output Scale Factor[7:0]								
	[47:40]	Phase Offset Word[15:8]								
	[39:32]	Phase Offset Word[7:0]								
	[31:24]	Frequency Tuning Word[31:24]								
	[23:16]	Frequency Tuning Word[23:16]								
	[15:8]	Frequency Tuning Word[15:8]								
	[7:0]	Frequency Tuning Word[7:0]								
RAM Register (0x16)	[63:56]	RAM Word[31:0]								
GPIO Configuration Register (0x18)	[55:48]	GPIO Configuration[15:0]								
GPIO Data Register (0x19)	[47:40]	GPIO Data[15:0]								

REGISTER BIT DESCRIPTIONS

The serial I/O port registers span an address range of 0 to 25 (0x00 to 0x19 in hexadecimal notation). This represents a total of 26 registers. However, six of these registers are unused, yielding a total of 20 available registers. The unused registers are 7, 8, 11 to 13, and 23 (0x07 to 0x08, 0x0B to 0x0D, and 0x17).

The number of bytes assigned to the registers varies. That is, the registers are not of uniform depth; each contains the number of bytes necessary for its particular function. Additionally, the registers are assigned names according to their functionality. In some cases, a register is given a mnemonic descriptor. For example, the register at Serial Address 0x00 is named Control Function Register 1 and is assigned the mnemonic CFR1.

The following section provides a detailed description of each bit in the MCD9957 register map. For cases in which a group of bits serves a specific function, the entire group is considered as a binary word and described in aggregate.

This section is organized in sequential order of the serial addresses of the registers. Following each subheading are the individual bit descriptions for that particular register. The location of the bit(s) in the register are indicated by [A] or [A:B], where A and B are bit numbers. The notation, [A:B], specifies a range of bits from most significant to least significant bit position. For example, [5:2] means bit positions 5 down to 2, inclusive, with Bit 0 identifying the LSB of the register.

Unless otherwise stated, programmed bits are not transferred to their internal destinations until the assertion of an I/O update or profile change.

Control Function Register 1 (CFR1)

Address 0x00, four bytes are assigned to this register.

Table 8 . Bit Descriptions for CFR1 Register

Bit (s)	Mnemonic	Description
31	RAM Enable	0: disables RAM playback functionality (default). 1: enables RAM playback functionality.
[30:29]	Open	
28	RAM Playback Destination	Ineffective unless CFR1, Bit 31 = 1. 0: RAM playback data routed to baseband scaling multipliers (default). 1: RAM playback data routed to baseband I/Q data path.
[27:26]	Open	
[25:24]	Operating Mode	00: quadrature modulation mode (default). 01: single tone mode. 1x: interpolating DAC mode.
23	Manual OSK External Control	Ineffective unless CFR1[9:8] = 10b. 0: OSK pin inoperative (default). 1: OSK pin enabled for manual OSK control (see the Output Shift Keying (OSK) section).
22	Inverse Sinc Filter Enable	0: inverse sinc filter bypassed (default). 1: inverse sinc filter active.
21	Clear CCI	The serial I/O port controller automatically clears this bit. This operation requires several internal clock cycles to complete, during which time the data supplied to the CCI input by the baseband signal chain is ignored. The inputs are forced to all zeros to flush the CCI data path, after which the CCI accumulators are reset. 0: normal operation of the CCI filter (default). 1: initiates an asynchronous reset of the accumulators in the CCI filter.
[20:17]	Open	
16	Select DDS Sine Output	Ineffective unless CFR1[25:24] = 01b. 0: cosine output of the DDS is selected (default). 1: sine output of the DDS is selected.
[15:14]	Open	
13	Autoclear Phase Accumulator	0: normal operation of the DDS phase accumulator (default). 1: synchronously resets the DDS phase accumulator any time I/O_UPDATE is asserted or a profile change occurs.
12	Open	
11	Clear Phase Accumulator	0: normal operation of the DDS phase accumulator (default). 1: asynchronous, static reset of the DDS phase accumulator.
10	Load ARR at I/O Update	0: normal operation of the OSK amplitude ramp rate timer (default). 1: OSK amplitude ramp rate timer reloaded any time I/O_UPDATE is asserted or a profile change occurs.

Bit (s)	Mnemonic	Description
9	OSK (Output Shift Keying) Enable	0: OSK disabled (default). 1: OSK enabled.
8	Select Auto-OSK	Ineffective unless CFR1, Bit 9 = 1. 0: manual OSK enabled (default). 1: automatic OSK enabled.
7	Digital Power-Down	This bit is effective without the need for an I/O update. 0: clock signals to the digital core are active (default). 1: clock signals to the digital core are disabled.
6	DAC Power-Down	0: DAC clock signals and bias circuits are active (default). 1: DAC clock signals and bias circuits are disabled.
5	REFCLK Input Power-Down	This bit is effective without the need for an I/O update. 0: REFCLK input circuits and PLL are active (default). 1: REFCLK input circuits and PLL are disabled.
4	Auxiliary DAC Power-Down	0: auxiliary DAC clock signals and bias circuits are active (default). 1: auxiliary DAC clock signals and bias circuits are disabled.
3	External Power-Down Control	0: assertion of the EXT_PWR_DWN pin affects full power-down (default). 1: assertion of the EXT_PWR_DWN pin affects fast recovery power-down.
2	Auto Power-Down Enable	Ineffective when CFR1[25:24] = 01b. 0: disable power-down (default). 1: when the TxENABLE pin is Logic 0, the baseband signal processing chain is flushed of residual data and the clocks are automatically stopped. Clocks restart when the TxENABLE pin is a Logic 1.
1	SDIO Input Only	0: configures the SDIO pin for bidirectional operation; 2-wire serial programming mode (default). 1: configures the serial data I/O pin (SDIO) as an input only pin; 3-wire serial programming mode.
0	LSB First	0: configures the serial I/O port for MSB first format (default). 1: configures the serial I/O port for LSB first format.

Control Function Register 2 (CFR2)

Address 0x01, four bytes are assigned to this register.

Table 9. Bit Descriptions for CFR2 Register

Bit (s)	Mnemonic	Description
31	Blackfin Interface Mode Active	Valid only when CFR1[25:24] = 00b (quadrature modulation mode). 0: Pin D[17:0] configured as an 18-bit parallel port (default). 1: Pin D[5:4] configured as a dual serial port compatible with the Blackfin serial interface. Pin D[17:6] and Pin D[3:0] become available as a 16-bit GPIO port.
30	Blackfin Bit Order	Valid only when CFR2, Bit 31 = 1. 0: the dual serial port (BFI) configured for MSB first operation (default). 1: the dual serial port (BFI) configured for LSB first operation.
29	Blackfin Early Frame Sync Enable	Valid only when CFR2, Bit 31 = 1. 0: the dual serial port (BFI) configured to be compatible with Blackfin late frame sync operation (default). 1: the dual serial port (BFI) configured to be compatible with Blackfin early frame sync operation.
[28:25]	Open	
24	Enable Profile Registers as ASF Source	Valid only when CFR1[25:24] = 01b (single tone mode) and CFR1, Bit 9 = 0 (OSK disabled). 0: amplitude scale factor bypassed (unity gain). 1: the active profile register determines the amplitude scale factor.
23	Internal I/O Update Active	This bit is effective without the need for an I/O update. 0: serial I/O programming is synchronized with external assertion of the I/O_UPDATE pin, which is configured as an input pin (default). 1: serial I/O programming is synchronized with an internally generated I/O update signal (the internally generated signal appears at the I/O_UPDATE pin, which is configured as an output pin).

Bit (s)	Mnemonic	Description
22	SYNC_CLK Enable	0: the SYNC_CLK pin is disabled; static Logic 0 output. 1: the SYNC_CLK pin generates a clock signal at ¼ f_{SYSCLK}; use of synchronization of the serial I/O port (default).
[21:17]	Open	
16	Read Effective FTW	0: a serial I/O port read operation of the FTW register reports the contents of the FTW register (default). 1: a serial I/O port read operation of the FTW register reports the actual 32-bit word appearing at the input to the DDS phase accumulator.
[15:14]	I/O Update Rate Control	Ineffective unless CFR2, Bit 23 = 1. Sets the prescale ratio of the divider that clocks the I/O update timer as follows: 00: divide by 1 (default). 01: divide by 2. 10: divide by 4. 11: divide by 8.
13	PDCLK Rate Control	Ineffective unless CFR2, Bit 31 = 0 and CFR1[25:24] = 00b. 0: PDCLK operates at the input data rate (default). 1: PDCLK operates at ½ the input data rate; useful for maintaining a consistent relationship between I/Q words at the parallel data port and the internal clocks of the baseband signal processing chain.
12	Data Format	0: the data-words applied to Pin D[17:0] are expected to be coded as twos complement (default). 1: the data-words applied to Pin D[17:0] are expected to be coded as offset binary.
11	PDCLK Enable	0: the PDCLK pin is disabled and forced to a static Logic 0 state; the internal clock signal continues to operate and provide timing to the data assembler. 1: the internal PDCLK signal appears at the PDCLK pin (default).
10	PDCLK Invert	0: normal PDCLK polarity; Q-data associated with Logic 1, I-data with Logic 0 (default). 1: inverted PDCLK polarity.
9	TxENABLE Invert	0: normal TxENABLE polarity; Logic 0 is standby, Logic 1 is transmit (default). 1: inverted TxENABLE polarity; Logic 0 is transmit, Logic 1 is standby.
8	Q-First Data Pairing	0: an I/Q data pair is delivered as I-data first, followed by Q-data (default). 1: an I/Q data pair is delivered as Q-data first, followed by I-data.
7	Match Dealy Enable	0:DDS amplitude,phase and frequency change synchronization application outputs in the order listed(default) 1:DDS ampiltude,phase and frequency change synchronization application outputs.
6	Data Assembler Hold Last Value	Ineffective when CFR1[25:24] = 01b. 0: when the TxENABLE pin is false, the data assembler ignores the input data and internally forces zeros on the baseband signal path (default). 1: when the TxENABLE pin is false, the data assembler ignores the input data and internally forces the last value received on the baseband signal path.
5	Sync Timing Validation Disable	0: enables the setup and hold validation circuit to take a measurement; the measurement result appears at the SYNC_SMP_ERR pin; a Logic 1 at this pin indicates a potential setup/hold violation whereas a Logic 0 indicates that a setup/hold violation has not been detected; the measurement result is latched and held until this bit is set to a Logic 1. 1: resets the setup and hold validation measurement circuit forcing the SYNC_SMP_ERR pin to a static Logic 0 condition (default); the measurement circuit is effectively disabled until this bit is restored to a Logic 0 state.
[4:0]	Open	

Control Function Register 3 (CFR3)

Address 0x02, four bytes are assigned to this register.

Table 10. Bit Descriptions for CFR3 Register

Bit (s)	Mnemonic	Description
[31:30]	Open	
[29:28]	DRV0	Controls REFCLK_OUT pin; default is 01b.
27	Open	
[26:24]	VCO SEL	Selects frequency band of the VCO in the REFCLK PLL ; default is 111b.
[23:22]	Open	
[21:19]	I_{CP}	Selects the charge pump current in the REFCLK PLL ; default is 111b.
[18:16]	Open	
15	REFCLK Input Divider Bypass	0: input divider is selected (default). 1: input divider is bypassed.
14	REFCLK Input Divider ResetB	0: input divider is reset. 1: input divider operates normally (default).
[13:9]	Open	
8	PLL Enable	0: REFCLK PLL bypassed (default). 1: REFCLK PLL enabled.
[7:1]	N	This 7-bit number is divide modulus of the REFCLK PLL feedback divider; default is 0000000b.
0	Open	

Auxiliary DAC Control Register

Address 0x03, four bytes are assigned to this register.

Table 11. Bit Descriptions for Auxiliary DAC Control Register

Bit(s)	Mnemonic	Description
[31:8]	Open	
[7:0]	FSC	This 8-bit number controls the full-scale output current of the main DAC (see the Auxiliary DAC section); default is 0xFF.

I/O Update Rate Register

Address 0x04, four bytes are assigned to this register. This register is effective without the need for an I/O update.

Table 12. Bit Descriptions for I/O Update Rate Register5

Bit(s)	Mnemonic	Description
[31:0]	I/O Update Rate	Ineffective unless CFR2, Bit 23 = 1. This 32-bit number controls the automatic I/O update rate (see the Automatic I/O Update section); default is 0xFFFFFFFF.

RAM Segment Register 0

Address 0x05, six bytes are assigned to this register. This register is effective without the need for an I/O update. This register is only active if CFR1, Bit 31 = 1 and there is a Logic 0 to Logic 1 transition on the RT pin.

Table 13. Bit Descriptions for RAM Segment Register 0

Bit(s)	Mnemonic	Description
[47:32]	RAM Address Step Rate 0	This 16-bit number controls the rate at which the RAM state machine steps through the specified RAM address range.
[31:22]	RAM End Address 0	This 10-bit number identifies the ending address for the RAM state machine.
[21:16]	Open	
[15:6]	RAM Start Address 0	This 10-bit number identifies the starting address for the RAM state machine.
[5:3]	Open	
[2:0]	RAM Playback Mode 0	This 3-bit number identifies the playback mode for the RAM state machine (see Table 5).

RAM Segment Register 1

Address 0x06, six bytes are assigned to this register. This register is only active if CFR1, Bit 31 = 1 and there is a Logic 1 to Logic 0 transition on the RT pin.

Table 14. Bit Descriptions for RAM Segment Register 1

Bit(s)	Mnemonic	Description
[47:32]	RAM Address Step Rate 1	This 16-bit number controls the rate at which the RAM state machine steps through the specified RAM address range.
[31:22]	RAM End Address 1	This 10-bit number identifies the ending address for the RAM state machine.
[21:16]	Open	
[15:6]	RAM Start Address 1	This 10-bit number identifies the starting address for the RAM state machine.
[5:3]	Open	
[2:0]	RAM Playback Mode 1	This 3-bit number identifies the playback mode for the RAM state machine (see Table 5).

Amplitude Scale Factor (ASF) Register

Address 0x09, four bytes are assigned to this register. This register is only active if CFR1, Bit 9 = 1.

Table 15. Bit Descriptions for ASF Register

Bit(s)	Mnemonic	Description
[31:16]	Amplitude Ramp Rate	Ineffective unless CFR1, Bit 8 = 1. This 16-bit number controls the rate at which the OSK controller updates amplitude changes to the DDS.
[15:2]	Amplitude Scale Factor	If CFR1, Bit 8 = 0 and CFR1, Bit 23 = 0, then this 14-bit number is the amplitude scale factor for the DDS. If CFR1, Bit 8 = 0 and CFR1, Bit 23 = 1, then this 14-bit number is the amplitude scale factor for the DDS when the OSK pin is Logic 1. If CFR1, Bit 8 = 1, then this 14-bit number sets a ceiling on the maximum allowable amplitude scale factor for the DDS.
[1:0]	Amplitude Step Size	Ineffective unless CFR1, Bit 8 = 1. This 2-bit number controls the step size for amplitude changes to the DDS (see Table 9).

Multichip Sync Register

Address 0x0A, four bytes are assigned to this register.

Table 16. Bit Descriptions for the Multichip Sync Register

Bit(s)	Mnemonic	Description
[31:28]	Sync Validation Delay	Default is 0000b. This 4-bit number sets the timing skew (in ~75 ps increments) between SYSCLK and the delayed sync-in signal for the synchronization validation block in the synchronization receiver.
27	Sync Receiver Enable	0: synchronization clock receiver disabled (default). 1: synchronization clock receiver enabled.
26	Sync Generator Enable	0: synchronization clock generator disabled (default). 1: synchronization clock generator enabled.
25	Sync Generator Polarity	0: synchronization clock generator coincident with the rising edge of the system clock (default). 1: synchronization clock generator coincident with the falling edge of the system clock.
24	Open	
[23:18]	Sync State Preset Value	Default is 000000b. This 6-bit number is the state that the internal clock generator assumes when it receives a sync pulse.
[17:16]	Open	
[15:11]	Sync Generator Delay	Default is 00000b. This 5-bit number sets the output delay (in ~75 ps increments) of the synchronization generator.
[10:8]	Open	
[7:3]	Sync Receiver Delay	Default is 00000b. This 5-bit number sets the delay input delay (in ~75 ps increments) of the synchronization receiver.
[2:0]	Open	

PROFILE REGISTERS

There are eight consecutive serial I/O addresses (0x0E to 0x15) dedicated to device profiles. All eight profile registers are either single tone profiles or QDUC profiles depending on the device operating mode specified by CFR1[25:24]. During operation, the active profile register is determined via the external PROFILE2, PROFILE1, and PROFILE0 pins.

Single tone profiles control: DDS frequency (32 bits), DDS phase offset (16 bits), and DDS amplitude scaling (14 bits).

QDUC profiles control: DDS frequency (32 bits), DDS phase offset (16 bits), output amplitude scaling (8 bits), CCI filter interpolation factor, inverse CCI bypass, and spectral invert. The QDUC profiles also selectively apply to the interpolating DAC operating mode: only output scaling, CCI filter interpolation factor, and inverse CCI bypass apply; all others (DDS frequency, output amplitude scaling, and spectral invert) are ignored.

Profile[7:0] Register—Single Tone

Address 0x0E to 0x15, eight bytes are assigned to this register.

Table 17. Bit Descriptions for Profile[7:0] Registers—Single Tone

Bit(s)	Mnemonic	Description
[63:62]	Open	
[61:48]	Amplitude Scale Factor	This 14-bit number controls the DDS output amplitude.
[47:32]	Phase Offset Word	This 16-bit number controls the DDS phase offset.
[31:0]	Frequency Tuning Word	This 32-bit number controls the DDS frequency.

Profile[7:0] Register—QDUC

Address 0x0E to 0x15, eight bytes are assigned to this register.

Table 18. Bit Descriptions for Profile[7:0] Registers—QDUC

Bit(s)	Mnemonic	Description
[63:58]	CC Interpolation Rate	This 6-bit number is the rate interpolation factor for the CCI filter.
57	Spectral Invert	0: the modulator output takes the form: I(t) × cos(ct) – Q(t) × sin(ct).
		1: the modulator output takes the form: I(t) × cos(ct) + Q(t) × sin(ct).
56	Inverse CCI Bypass	0: the inverse CCI filter is enabled.
		1: the inverse CCI filter is bypassed.
[55:48]	Output Scale Factor	This 8-bit number controls the output amplitude.
[47:32]	Phase Offset Word	This 16-bit number controls the DDS phase offset.
[31:0]	Frequency Tuning Word	This 32-bit number controls the DDS frequency.

RAM Register

Address 0x16, four bytes are assigned to this register.

Table 19. Bit Descriptions for RAM Register

Bit(s)	Mnemonic	Description
[31:0]	RAM Word	The number of 32-bit words written to RAM is defined by the start and end address in RAM Segment Register 0 or RAM Segment Register 1.

GPIO Configuration Register

Address 0x18, two bytes are assigned to this register.

Table 20. Bit Descriptions for GPIO Configuration Register

Bit(s)	Mnemonic	Description
[15:0]	GPIO Configuration	See the General-Purpose I/O (GPIO) Port section for details.

GPIO Data Register

Address 0x19, two bytes are assigned to this register.

Table 21Bit Descriptions for GPIO Data Register

Bit(s)	Mnemonic	Description
[15:0]	GPIO Data	Read or write based on the contents of the GPIO Configuration register. See the General-Purpose I/O (GPIO) Port section for details.

Table 2 2 .REFCLK_OUT Buffer Control

(CFR3[29:28])	REFCLK_OUT Buffer
00	Disabled
01	Low Output Current
10	Medium Output Current
11	High Output Current

Table 23.VCO Range Bit Setting

VCO SEL Bit(CFR3[26:24])	REFCLK_OUT Buffer
000	VCO0
001	VCO1
010	VCO2
011	VCO3
100	VCO4
101	VCO5
110	PLL is passed
111	PLL is passed

Table 24.PLL Charge Pump Current

CFR3[29:28])	REFCLK_OUT Buffer
000	212
001	237
010	262
011	287
100	312
101	337
110	363
111	387

Table 25.OSK Amplitude Step

ASF[1:0]	RAMPLITUDE STEP
00	1
01	2
10	4
11	8

OUTLINE DIMENSIONS

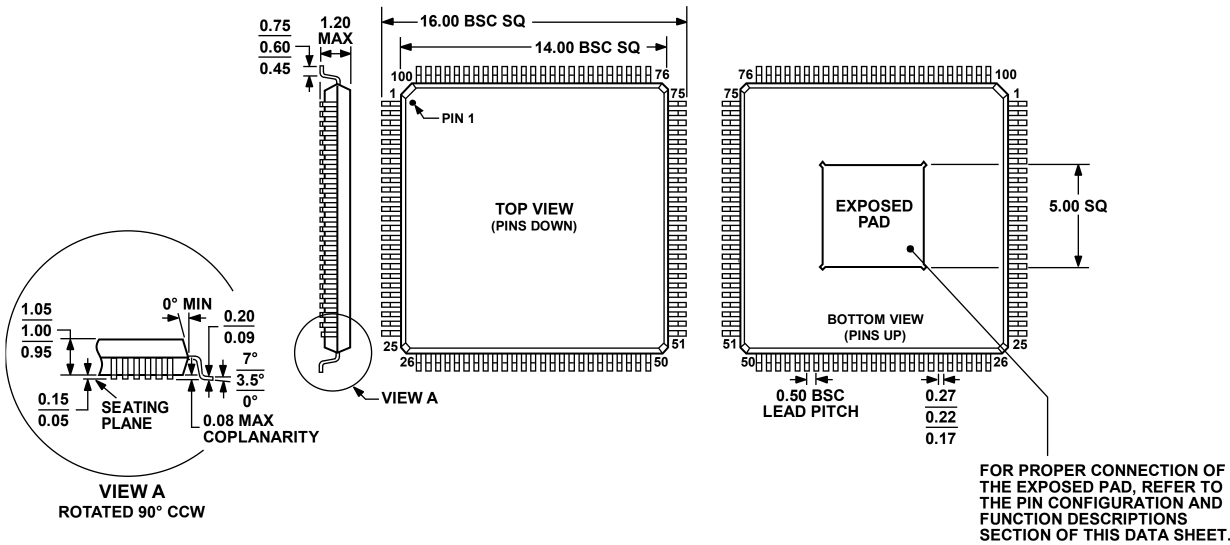


Figure 7. 100-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-100-4)
Dimensions shown in millimeters

Table 25. ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
MCD9957TFP	−40°C to +85°C	TQFP-100	Tray-900

[1] Z = RoHS Compliant Part.