

FEATURES

- High dynamic range, dual digital-to-analog converters (DACs)
- Low noise and intermodulation distortion
- Single carrier W-CDMA ACLR = 80 dBc at 61.55MHz
- Innovative switching output stage permits useable outputs beyond Nyquist frequency
- LVC MOS inputs with dual-port or optional interleaved single-port operation
- Differential analog current outputs are programmable from 8.6 mA to 31.7 mA full-scale
- Auxiliary 10-bit current DACs with source/sink capability for external offset nulling
- Internal 1.2 V precision reference voltage source
- Operates from 1.8 V and 3.3 V supplies
- 320 mW power dissipation
- Small footprint, RoHS-compliant, 72-lead LFCSP

APPLICATIONS

- Wireless infrastructure
 - W-CDMA, CDMA2000, TD-SCDMA, WiMAX
- Wideband communications: LMDS/MMDS, point-to-point
- Instrumentation
 - Radio frequency (RF) signal generators, arbitrary waveform generators

GENERAL DESCRIPTION

The MCD9747 are pin-compatible, high dynamic range, dual DACs with 16-bit resolutions and sample rates of up to 250 MSPS. The devices include specific features for direct conversion transmit applications, including gain and offset compensation, and they interface seamlessly with analog quadrature modulators. A proprietary, dynamic output architecture permits synthesis of analog outputs even above Nyquist by shifting energy away from the fundamental and into the image frequency.

A serial peripheral interface (SPI) port provides full programmability. In addition, some pin-programmable features are offered for those applications without a controller.

PRODUCT HIGHLIGHTS

1. Low noise and intermodulation distortion (IMD) enables high quality synthesis of wideband signals.
2. Proprietary switching output for enhanced dynamic performance.
3. Programmable current outputs and dual auxiliary DACs provide flexibility and system enhancements.

FUNCTIONAL BLOCK DIAGRAM

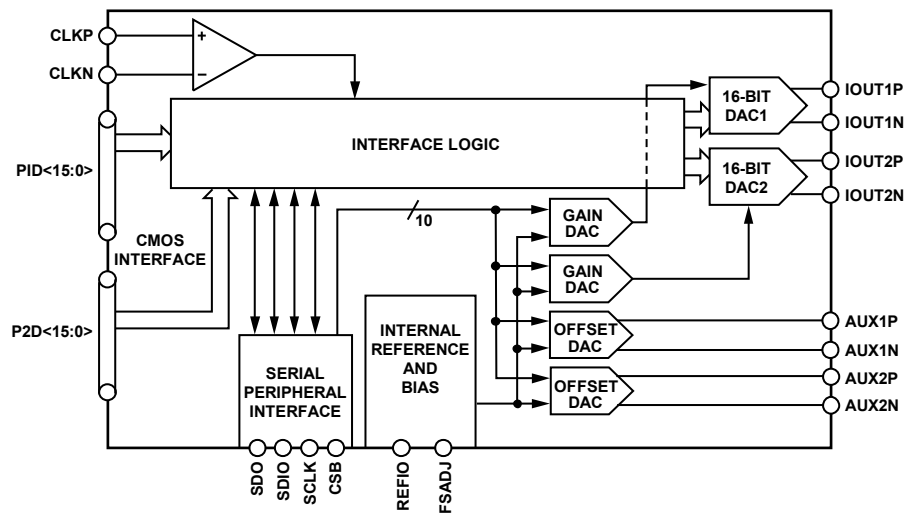


Figure 1.

DC SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 1.

Parameter	MCD9747			Unit
	Min	Typ	Max	
RESOLUTION		16		Bits
ACCURACY				
Differential Nonlinearity (DNL)		±2.0		LSB
Integral Nonlinearity (INL)		±4.0		LSB
MAIN DAC OUTPUTS				
Offset Error		±0.001		%FSR
Offset Error Temperature Coefficient		0.1		ppm/°C
Gain Error		±2.0		%FSR
Gain Error Temperature Coefficient		100		ppm/°C
Gain Matching (DAC1 to DAC2)		±1.0		%FSR
Full-Scale Output Current	8.6		31.7	mA
Output Compliance Voltage	-1.0		+1.0	V
Output Resistance		10		MΩ
AUXILIARY DAC OUTPUTS				
Resolution		10		Bits
Full-Scale Output Current	-2.0		+2.0	mA
Output Compliance Voltage Range—Sink Current	0.8		1.6	V
Output Compliance Voltage Range—Source Current	0		1.6	V
Output Resistance		1		MΩ
Monotonicity	10			Bits
REFERENCE INPUT/OUTPUT				
Output Voltage		1.2		V
Output Voltage Temperature Coefficient		10		ppm/°C
External Input Voltage Range	1.15		1.3	V
Input or Output Resistance		5		kΩ
POWER SUPPLY VOLTAGES				
AVDD33, DVDD33	3.13		3.47	V
CVDD18, DVDD18	1.70		1.90	V
POWER SUPPLY CURRENTS				
I_{AVDD33}		56	60	mA
I_{DVDD33}		12	16	mA
I_{CVDD18}		18	22	mA
I_{DVDD18}		32	36	mA
POWER DISSIPATION				
$f_{DAC} = 250$ MSPS, $f_{OUT} = 20$ MHz		310	355	mW
DAC Outputs Disabled		125		mW
Full Device Power-Down		3		mW
OPERATING TEMPERATURE	-40		+85	°C

AC SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, AVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 2.

Parameter	MCD9747			Unit
	Min	Typ	Max	
SPURIOUS FREE DYNAMIC RANGE (SFDR)				
$f_{DAC} = 250$ MSPS, $f_{OUT} = 20$ MHz		83		dBc
$f_{DAC} = 250$ MSPS, $f_{OUT} = 70$ MHz		70.5		dBc
$f_{DAC} = 250$ MSPS, $f_{OUT} = 180$ MHz ¹		66		dBc
INTERMODULATION DISTORTION (IMD)				
$f_{DAC} = 250$ MSPS, $f_{OUT} = 20$ MHz		87		dBc
$f_{DAC} = 250$ MSPS, $f_{OUT} = 70$ MHz		81		dBc
$f_{DAC} = 250$ MSPS, $f_{OUT} = 180$ MHz ¹		73		dBc
CROSSTALK				
$f_{DAC} = 250$ MSPS, $f_{OUT} = 20$ MHz		80		dBc
$f_{DAC} = 250$ MSPS, $f_{OUT} = 70$ MHz		80		dBc
$f_{DAC} = 250$ MSPS, $f_{OUT} = 180$ MHz ¹		80		dBc
ADJACENT CHANNEL LEAKAGE RATIO (ACLR) SINGLE CARRIER W-CDMA				
$f_{DAC} = 245.76$ MSPS, $f_{OUT} = 15.36$ MHz		82		dBc
$f_{DAC} = 245.76$ MSPS, $f_{OUT} = 61.44$ MHz		80		dBc
$f_{DAC} = 245.76$ MSPS, $f_{OUT} = 184.32$ MHz ¹		74		dBc
NOISE SPECTRAL DENSITY (NSD)				
$f_{DAC} = 245.76$ MSPS, $f_{OUT} = 15.36$ MHz		-164		dBm/Hz
$f_{DAC} = 245.76$ MSPS, $f_{OUT} = 61.44$ MHz		-161		dBm/Hz
$f_{DAC} = 245.76$ MSPS, $f_{OUT} = 184.32$ MHz ¹		-159		dBm/Hz

¹ Mix mode.

DIGITAL AND TIMING SPECIFICATIONS

T_{MIN} to T_{MAX} , AVDD33 = 3.3 V, DVDD33 = 3.3 V, DVDD18 = 1.8 V, CVDD18 = 1.8 V, I_{FS} = 20 mA, full-scale digital input, maximum sample rate, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
DAC CLOCK INPUTS (CLKP, CLKN)				
Differential Peak-to-Peak Voltage	400	800	1600	mV
Single-Ended Peak-to-Peak Voltage			800	mV
Common-Mode Voltage	300	400	500	mV
Input Current			1	μ A
Input Frequency			250	MHz
DATA CLOCK OUTPUT (DCO)				
Output Voltage High	2.4			V
Output Voltage Low			0.4	V
Output Current			10	mA
DAC Clock to Data Clock Output Delay (t_{DCO})	2.0	2.2	2.8	ns
DATA PORT INPUTS				
Input Voltage High	2.0			V
Input Voltage Low			0.8	V
Input Current			1	μ A
Data to DAC Clock Setup Time (t_{DBS} Dual-Port Mode)	400			ps
Data to DAC Clock Hold Time (t_{DBH} Dual-Port Mode)	1200			ps
DAC Clock to Analog Output Data Latency (Dual-Port Mode)			7	Cycles
Data or IQSEL Input to DAC Clock Setup Time (t_{DBS} Single-Port Mode)	400			ps
Data or IQSEL Input to DAC Clock Hold Time (t_{DBH} Single-Port Mode)	1200			ps
DAC Clock to Analog Output Data Latency (Single-Port Mode)			8	Cycles
SERIAL PERIPHERAL INTERFACE				
SCLK Frequency (f_{SCLK})			40	MHz
SCLK Pulse Width High (t_{PWH})	10			ns
SCLK Pulse Width Low (t_{PWL})	10			ns
CSB to SCLK Setup Time (t_s)	1			ns
CSB to SCLK Hold Time (t_H)	0			ns
SDIO to SCLK Setup Time (t_{DS})	1			ns
SDIO to SCLK Hold Time (t_{DH})	0			ns
SCLK to SDIO/SDO Data Valid Time (t_{DV})			1	ns
RESET Pulse Width High	10			ns
WAKE-UP TIME AND OUTPUT LATENCY				
From DAC Outputs Disabled		200		μ s
From Full Device Power-Down		1200		μ s
DAC Clock to Analog Output Latency (Dual-Port Mode)		7		Cycles
DAC Clock to Analog Output Latency (Single-Port Mode)		8		Cycles

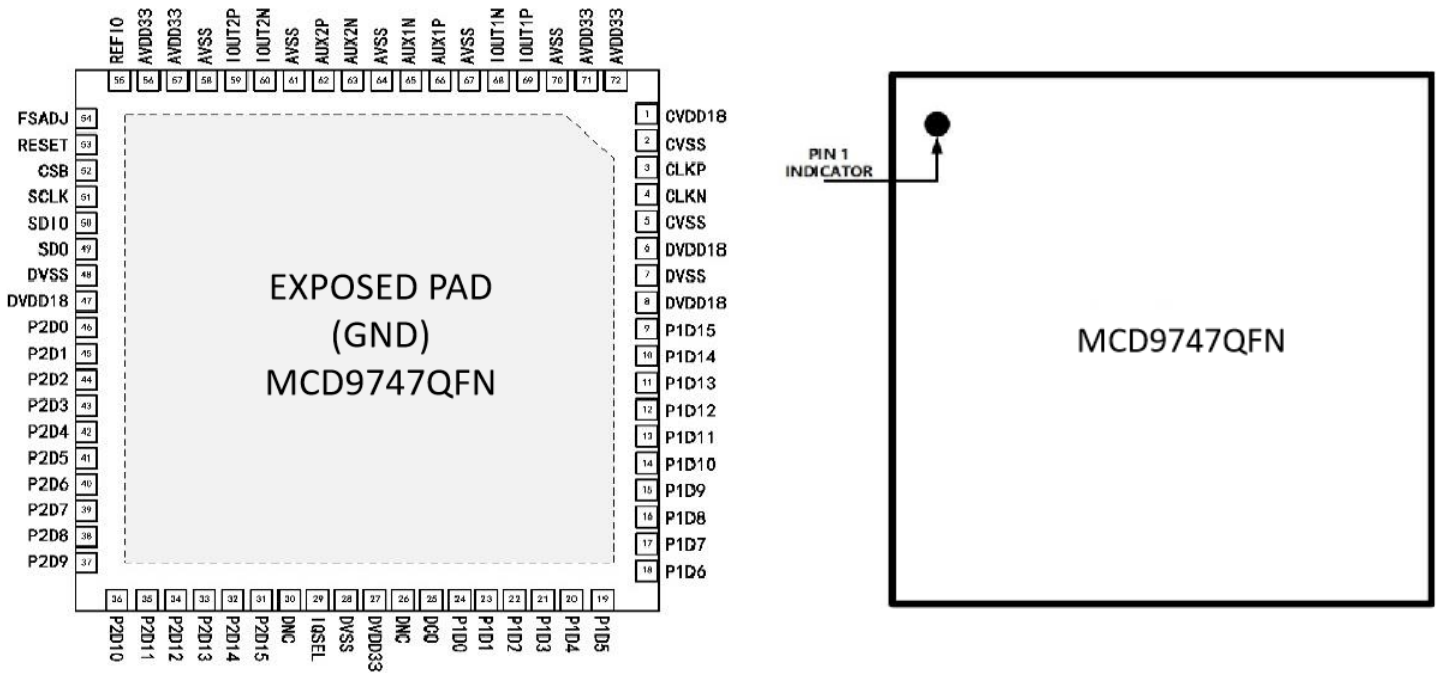


Figure 2. MCD9747 Pin Configuration

Table 4. MCD9747 Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 6	CVDD18	Clock Supply Voltage (1.8 V).
2, 5	CVSS	Clock Supply Common (0 V).
3	CLKP	Differential DAC Clock Input.
4	CLKN	Complementary Differential DAC Clock Input.
7, 28, 48	DVSS	Digital Supply Common (0 V).
8, 47	DVDD18	Digital Core Supply Voltage (1.8 V).
9 to 24	P1D15, P1D14, P1D13, P1D12, P1D11, P1D10, P1D9, P1D8, P1D7, P1D6, P1D5, P1D4, P1D3, P1D2, P1D1, P1D0	Port 1 Data Bit Inputs.
25	DCO	Data Clock Output. Use to clock data source.
26, 30	DNC	Do Not Connect. Do not connect to these pins.
27	DVDD33	Digital Input/Output Supply Voltage (3.3 V).
29	IQSEL	I/Q Framing Signal for Single-Port Mode Operation.
31 to 46	P2D15, P2D14, P2D13, P2D12, P2D11, P2D10, P2D9, P2D8, P2D7, P2D6, P2D5, P2D4, P2D3, P2D2, P2D1, P2D0	Port 2 Data Bit Inputs.
49	SDO	Serial Peripheral Interface Data Output.
50	SDIO	Serial Peripheral Interface Data Input and Optional Data Output.
51	SCLK	Serial Peripheral Interface Clock Input.
52	CSB	Serial Peripheral Interface Chip Select Input. Active low.
53	RESET	Hardware Reset. Active high.
54	FSADJ	Full-Scale Current Output Adjust. Connect a 10 kΩ resistor to AVSS.
55	REFIO	Reference Input/Output. 1.2V Output. Connect a 0.1 μF capacitor to AVSS.
56, 57, 71, 72	AVDD33	Analog Supply Voltage (3.3 V).
58, 61, 64, 67, 70	AVSS	Analog Supply Common (0 V).

Pin No.	Mnemonic	Description
59	IOOUT2P	DAC2 Current Output. Sources full-scale current when input data bits are all 1.
60	IOOUT2N	Complementary DAC2 Current Output. Sources full-scale current when data bits are all 0.
62	AUX2P	Auxiliary DAC2 Default Current Output Pin.
63	AUX2N	Auxiliary DAC2 Optional Output Pin. Enable through SPI.
65	AUX1N	Auxiliary DAC1 Optional Output Pin. Enable through SPI.
66	AUX1P	Auxiliary DAC1 Default Current Output Pin.
68	IOOUT1N	Complementary DAC1 Current Output. Sources full-scale current when data bits are all 0.
69	IOOUT1P	DAC1 Current Output. Sources full-scale current when data bits are all 1.
	EPAD	Exposed Thermal Pad. The exposed thermal pad must be soldered to copper pour on top surface of PCB for mechanical stability and must be electrically tied to low impedance GND plane for low noise performance.

THEORY OF OPERATION

SPI PORT

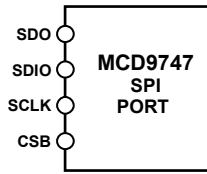


Figure 21. SPI Port

The SPI port is a flexible, synchronous serial communications port allowing easy interfacing to many industry-standard microcontrollers and microprocessors.

The interface allows read and write access to all registers that configure the MCD9747. Single or multiple byte transfers are supported. Accomplish serial data input/output through a single bidirectional pin (SDIO) or through two unidirectional pins (SDIO/SDO).

The serial port configuration is controlled by Register 0x00, Bits[7]. It is important to note that any change made to the serial port configuration occurs immediately upon writing to the last bit of this byte. Therefore, it is possible with a multibyte transfer to write to this register and change the configuration in the middle of a communication cycle. Take care to compensate for the new configuration within the remaining bytes of the current communication cycle.

GENERAL OPERATION OF THE SERIAL INTERFACE

There are two phases to any communication cycle with the MCD9747: Phase 1 and Phase 2.

Phase 1 is the instruction cycle, which writes an instruction byte into the device. This byte provides the serial port controller with information regarding Phase 2 of the communication cycle: the data transfer cycle.

The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and a reference register address for the first byte of the data transfer. A logic high on the CSB pin followed by a logic low resets the SPI port to its initial state and defines the start of the instruction cycle. From this point, the next eight rising SCLK edges define the eight bits of the instruction byte for the current communication cycle.

The remaining SCLK edges are for Phase 2 of the communication cycle, which is the data transfer between the serial port controller and the system controller. Phase 2 can be a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Using multibyte transfers is usually preferred although single-byte data transfers are useful to reduce CPU overhead or when only a single register access is required.

All serial port data transfers to and from the device in synchronization with the SCLK pin. Input data always latches on the rising edge of SCLK whereas output data is always valid after the falling edge of SCLK. Register contents change immediately upon writing to the last bit of each transfer byte.

When synchronization is lost, the device has the ability to terminate an input/output operation asynchronously whenever the CSB pin is taken to logic high. Any unwritten register content data is lost if the input/output operation is aborted. Taking CSB low then resets the serial port controller and restarts the communication cycle.

INSTRUCTION BYTE

The instruction byte contains the information shown in the following bit map.

MSB						LSB	
B7	B6	B5	B4	B3	B2	B1	B0
R/W	N1	N0	A4	A3	A2	A1	A0

Bit 7, R/W, determines whether a read or a write data transfer occurs after the instruction byte write. Logic high indicates a read operation. Logic 0 indicates a write operation.

Bits[6:5], N1 and N0, determine the number of bytes to be transferred during the data transfer cycle. The bits decode as shown in Table 5.

Table 5 . Byte Transfer Count

N1	N0	Description
0	0	Transfer one byte
0	1	Transfer two bytes
1	0	Transfer three bytes
1	1	Transfer four bytes

Bits[4:0], A4, A3, A2, A1, and A0, determine which register is accessed during the data transfer of the communications cycle. For multibyte transfers, this address is a starting or ending address depending on the current data transfer mode. For MSB-first format, the specified address is an ending address or the most significant address in the current cycle. The serial port controller internally generates the remaining register addresses for multiple byte data transfers by decrementing from the

specified address. For LSB-first format, the specified address is a beginning address or the least significant address in the current cycle. The serial port controller internally generates the remaining register addresses for multiple byte data transfers by incrementing from the specified address.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

Chip Select Bar (CSB)

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communication lines. CSB must stay low during the entire communication cycle. Incomplete data transfers abort anytime the CSB pin goes high. SDO and SDIO pins go to a high impedance state when this input is high.

Serial Clock (SCLK)

The serial clock pin synchronizes data to and from the device and runs the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Serial Data Input/Output (SDIO)

Data is always written into the device on this pin. However, SDIO can also function as a bidirectional data output line. Register 0x00, Bit 7 controls the configuration of this pin. The default is Logic 0, which configures the SDIO pin as unidirectional.

Serial Data Out (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. Register 0x00, Bit 7 controls the configuration of this pin. If this bit is set to a Logic 1, the SDO pin does not output data and is set to a high impedance state.

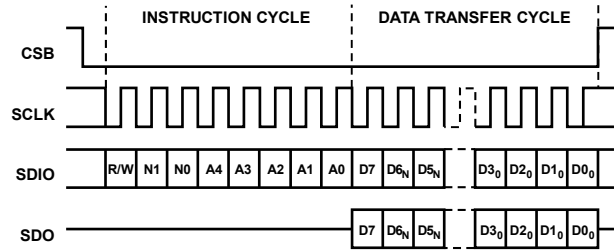


Figure 3. Serial Register Interface Timing—MSB First

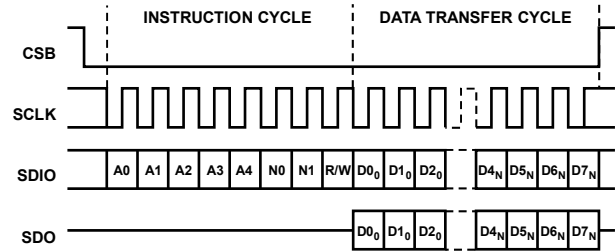


Figure 4. Serial Register Interface Timing—LSB First

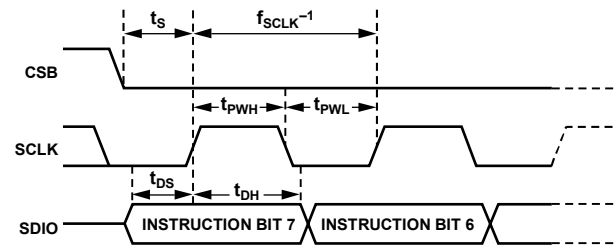


Figure 5. Timing Diagram for SPI Register Write

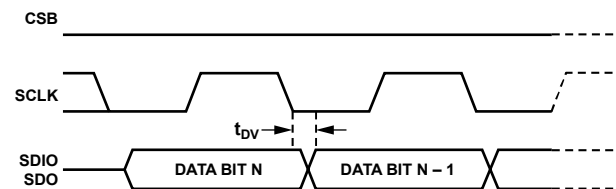


Figure 6. Timing Diagram for SPI Register Read

SPI REGISTER DESCRIPTIONS

Table 6.

Register	Address	Bit	Name	Description
SPI Control	0x00	7	SDIODIR	0 = operate SPI in 4-wire mode, SDIO pin operates as an input only 1 = operate SPI in 3-wire mode, SDIO pin operates as a bidirectional input/output line
		6	LSBFIRST	0 = LSBFIRST off, SPI serial data mode is MSB to LSB 1 = LSBFIRST on, SPI serial data mode is LSB to MSB
		5	SWRESET	0 = resume normal operation following software RESET 1 = software RESET; loads default values to all registers (except Register 0x00)
Data Control	0x02	7	DATYPE	0 = DAC input data is twos complement binary format 1 = DAC input data is unsigned binary format
		6	ONEPORT	0 = normal dual-port input mode 1 = optional single port input mode, interleaved data received on Port 1 only
		4	INVDCO	1 = inverts data clock output signal
Power Down	0x03	7	PD_DCO	1 = power down data clock output
		5	PD_AUX2	1 = power down AUX2 DAC
		4	PD_AUX1	1 = power down AUX1 DAC
		3	PD_BIAS	1 = power down reference voltage bias circuit
		2	PD_CLK	1 = power down DAC clock input circuit
		1	PD_DAC2	1 = power down DAC2 analog output
		0	PD_DAC1	1 = power down DAC1 analog output
DAC Mode Select	0x0A	3:2	DAC1MOD[1:0]	00 = selects normal mode, DAC1 01 = selects mix mode, DAC1 10 = selects return to zero mode, DAC1
		1:0	DAC2MOD[1:0]	00 = selects normal mode, DAC2 01 = selects mix mode, DAC2 10 = selects return to zero mode, DAC2
DAC1 Gain	0x0B	7:0	DAC1FSC[7:0]	DAC1 full-scale 10-bit adjustment word
	0x0C	1:0	DAC1FSC[9:8]	0x03FF = sets full-scale current to the maximum value of 31.66 mA 0x01F9 = sets full-scale current to the nominal value of 20.0 mA 0x0000 = sets full-scale current to the minimum value of 8.64 mA
AUX DAC1	0x0D	7:0	AUXDAC1[7:0]	Auxiliary DAC1 10-bit output current adjustment word
	0x0E	1:0	AUXDAC1[9:8]	0x03FF = sets output current magnitude to 2.0 mA 0x0200 = sets output current magnitude to 1.0 mA 0x0000 = sets output current magnitude to 0.0 mA
		7	AUX1PIN	1 = AUX1P output pin is active 0 = AUX1N output pin is active
	6	AUX1DIR	0 = configures AUX1 DAC output to source current 1 = configures AUX1 DAC output to sink current	
DAC2 Gain	0x0F	7:0	DAC2FSC[7:0]	DAC2 full-scale 10-bit adjustment word
	0x10	1:0	DAC2FSC[9:8]	0x03FF = sets full-scale current to the maximum value of 31.66 mA 0x01F9 = sets full-scale current to the nominal value of 20.0 mA 0x0000 = sets full-scale current to the minimum value of 8.64 mA
AUX DAC2	0x11	7:0	AUXDAC2[7:0]	Auxiliary DAC2 10-bit output current adjustment word
	0x12	1:0	AUXDAC2[9:8]	0x03FF = sets output current magnitude to 2.0 mA 0x0200 = sets output current to 1.0 mA 0x0000 = sets output current to 0.0 mA
		7	AUX2PIN	1 = AUX2P output pin is active 0 = AUX2N output pin is active
	6	AUX2DIR	0 = configures AUX2 DAC output to source current 1 = configures AUX2 DAC output to sink current	

DIGITAL INPUTS AND OUTPUTS

The [MCD9747](#) can operate in two data input modes: dual-port mode and single-port mode. For the default dual-port mode ($\text{ONEPORT} = 0$), each DAC receives data from a dedicated input port. In single-port mode ($\text{ONEPORT} = 1$), however, both DACs receive data from Port 1. In single-port mode, DAC1 and DAC2 data is interleaved and the IQSEL input steers data to the correct DAC.

In single-port mode, when the IQSEL input is high, Port 1 data is delivered to DAC1 and when IQSEL is low, Port 1 data is delivered to DAC2. The IQSEL input must always coincide and be time-aligned with the other data bus signals. In single-port mode, minimum setup and hold times apply to the IQSEL input as well as to the input data signals. In dual-port mode, the IQSEL input is ignored.

In dual-port mode, the data must be delivered at the sample rate (up to 250 MSPS). In single-port mode, data must be delivered at twice the sample rate. Because the data inputs function only up to 250 MSPS, it is only practical to operate the DAC clock at up to 125 MHz in single-port mode.

In both dual-port and single-port modes, a data clock output (DCO) signal is available as a fixed time base with which to stimulate data from an FPGA. This output signal always operates at the sample rate. It can be inverted by asserting the INVDCO bit.

INPUT DATA TIMING

With most DACs, signal-to-noise ratio (SNR) is a function of the relationship between the position of the clock edges and the point in time at which the input data changes. The [MCD9747](#) are rising edge triggered and thus exhibit greater SNR sensitivity when the data transition is close to this edge.

The specified minimum setup and hold times define a window of time, within each data period, where the data is sampled correctly. Users must position data to arrive relative to the DAC clock and well beyond the minimum setup and minimum hold times. This becomes increasingly more important at increasingly higher sample rates.

DUAL-PORT MODE TIMING

Figure 7 shows the timing diagram for the dual-port mode.

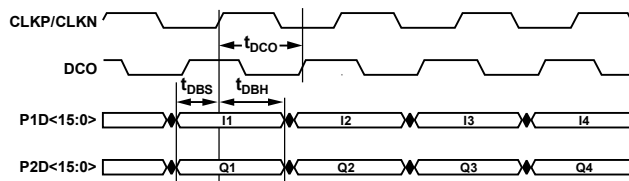


Figure 7. Data Interface Timing, Dual-Port Mode

In Figure 7, data samples for DAC1 are labeled Ix and data samples for DAC2 are labeled Qx. Note that the differential DAC clock input is shown in a logical sense (CLKP/CLKN). The data clock output is labeled DCO.

Setup and hold times are referenced to the positive transition of the DAC clock. Data must arrive at the input pins such that the minimum setup and hold times are met. Note that the data clock output has a fixed time delay from the DAC clock and may be a more convenient signal to use to confirm timing.

SINGLE-PORT MODE TIMING

Figure 8 shows the single-port mode timing diagram.

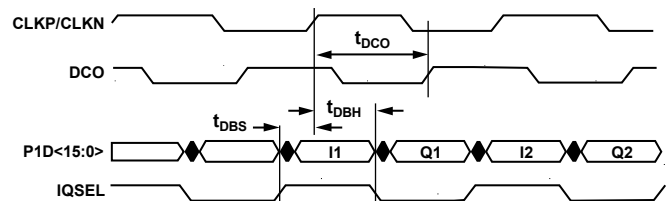


Figure 8. Data Interface Timing, Single-Port Mode

In single-port mode, data for both DACs is received on the Port 1 input bus. Ix and Qx data samples are interleaved and arrive twice as fast as in dual-port mode. Accompanying the data is the IQSEL input signal, which steers incoming data to its respective DAC. When IQSEL is high, data is steered to DAC1 and when IQSEL is low, data is steered to DAC2. IQSEL must coincide as well as be time-aligned with incoming data.

DRIVING THE DAC CLOCK INPUT

The DAC clock input requires a low jitter drive signal. It is a PMOS differential pair powered from the CVDD18 supply. Each pin can safely swing up to 800 mV p-p at a common-mode voltage of about 400 mV. Though these levels are not directly LVDS-compatible, CLKP and CLKN can be driven by an ac-coupled, dc-offset LVDS signal, as shown in Figure 9.

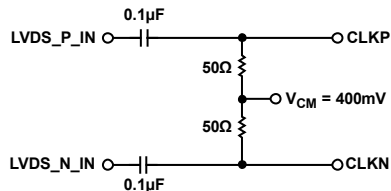


Figure 9. LVDS DAC Clock Drive Circuit

Using a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through an LVDS translator and then ac-coupled as described previously, or alternatively, it can be transformer-coupled and clamped, as shown in Figure 10.

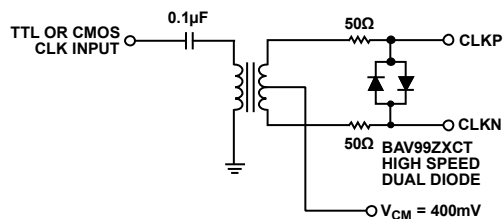


Figure 10. TTL or CMOS DAC Clock Drive Circuit

If a sine wave signal is available, it can be transformer-coupled directly to the DAC clock inputs, as shown in Figure 11.

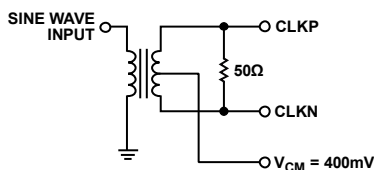


Figure 11. Sine Wave DAC Clock Drive Circuit

The 400 mV common-mode bias voltage can be derived from the CVDD18 supply through a simple divider network, as shown in Figure 12.

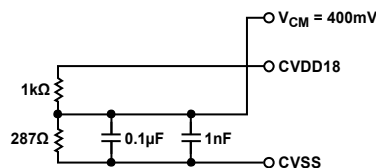


Figure 12. DAC Clock VCM Circuit

It is important to use CVDD18 and CVSS for any clock bias circuit as noise that is coupled onto the clock from another power supply is multiplied by the DAC input signal and degrades performance.

FULL-SCALE CURRENT GENERATION

The full-scale currents on DAC1 and DAC2 are functions of the current drawn through an external resistor connected to the FSADJ pin (Pin 54). The required value for this resistor is 10 kΩ. REFIO (Pin 55) must be bypassed to ground with a 0.1 μF capacitor.

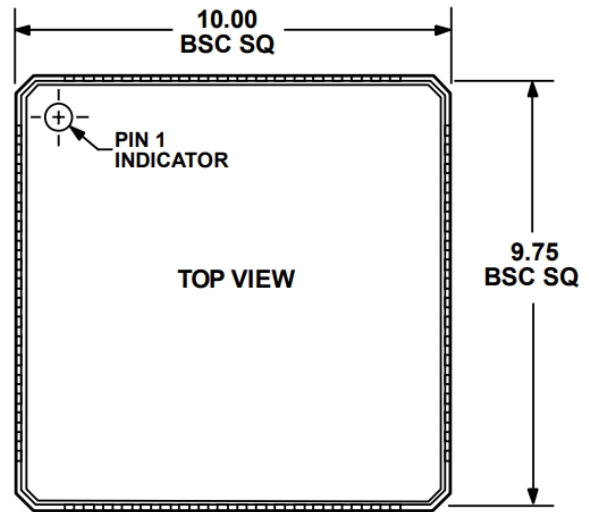
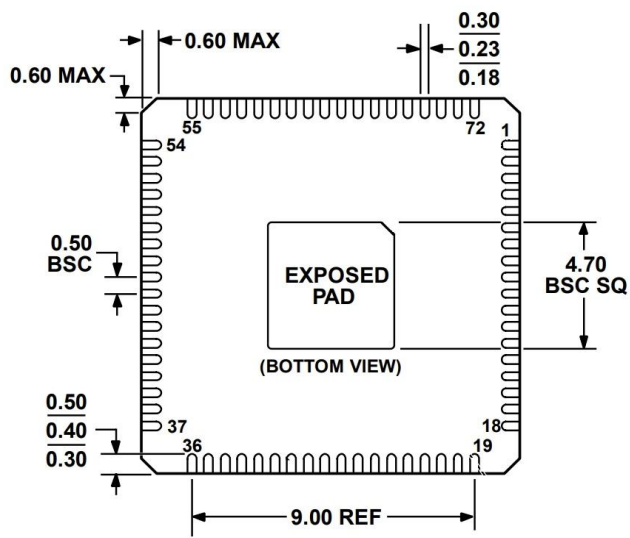
Internal current mirrors provide a means for adjusting the DAC full-scale currents. The gain for DAC1 and DAC2 can be adjusted independently by writing to the DAC1FSC[9:0] and DAC2FSC[9:0] register bits. The default value of 0x01F9 for the DAC gain registers gives an I_{FS} of 20 mA, where I_{FS} equals

$$I_{FS} = \frac{1.2 \text{ V}}{10,000} \times \left(72 + \left(\frac{3}{16} \times \text{DACn FSC} \right) \right)$$

OPERATIONAL MODE

The MCD9747 operates in three modes: Normal mode, Mixing mode, and Zero Return mode.

OUTLINE DIMENSIONS



ORDERING GUIDE

Model	Temperature Range	Package Description	Packing Method	ROHS
MCD9747LFP-250	-40°C to +85°C	72-QFN	168/Tray	Y