MCA1220 4-Channel, 2-kSPS, Low-Power, 24-Bit ADC with Integrated PGA and Reference

Features

- Low Current Consumption:
  As Low as 120 μA (typ) in Duty-Cycle Mode
- Wide Supply Range: 2.3 V to 5.5 V
- Programmable Gain: 1 V/V to 128 V/V
- Programmable Data Rates: Up to 2 kSPS
- Up to 20-Bits Effective Resolution
- Simultaneous 50-Hz and 60-Hz Rejection at 20 SPS with Single-Cycle Settling Digital Filter
- Two Differential or Four Single-Ended Inputs
- Dual Matched Programmable Current Sources: 10 μA to 1.5 mA
- Internal 2.048V Reference: 5 ppm/°C (typ) Drift
- Internal 2% Accurate Oscillator
- Internal Temperature Sensor:
  0.5°C (typ) Accuracy
- SPI-Compatible Interface (Mode 1)
- Package: 3.5-mm × 3.5-mm × 0.9-mm VQFN

Applications

- Temperature Sensor Measurements:
  - Thermistors
  - Thermocouples
  - Resistance Temperature Detectors (RTDs): 2-, 3-, or 4-Wire Types
- Resistive Bridge Sensor Measurements:
  - Pressure Sensors
  - Strain Gauges
  - Weigh Scales
- Portable Instrumentation
- Factory Automation and Process Control

Description

The MCA1220 is a precision, 24-bit, analog-to-digital converter (ADC) that offers many integrated features to reduce system cost and component count in applications measuring small sensor signals. The device features two differential or four single-ended inputs through a flexible input multiplexer (MUX), a low-noise, programmable gain amplifier (PGA), two programmable excitation current sources, a voltage reference, an oscillator, a low-side switch, and a precision temperature sensor.

The device can perform conversions at data rates up to 2000 samples-per-second (SPS) with single-cycle settling. At 20 SPS, the digital filter offers simultaneous 50-Hz and 60-Hz rejection for noisy industrial applications. The internal PGA offers gains up to 128 V/V. This PGA makes the MCA1220 ideally suited for applications measuring small sensor signals, such as resistance temperature detectors (RTDs), thermocouples, thermistors, and resistive bridge sensors. The device supports measurements of pseudo- or fully-differential signals when using the PGA. Alternatively, the device can be configured to bypass the internal PGA while still providing high input impedance and gains up to 4 V/V, allowing for single-ended measurements.

Power consumption is as low as 120 μA when operating in duty-cycle mode with the PGA disabled.

The MCA1220 is offered in a leadless VQFN-16 or a TSSOP-16 package and is specified over a temperature range of –40°C to +125°C.

Table 1.Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCA1220	VQFN (16)	3.50 mm × 3.50 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

K-Type Thermocouple Measurement

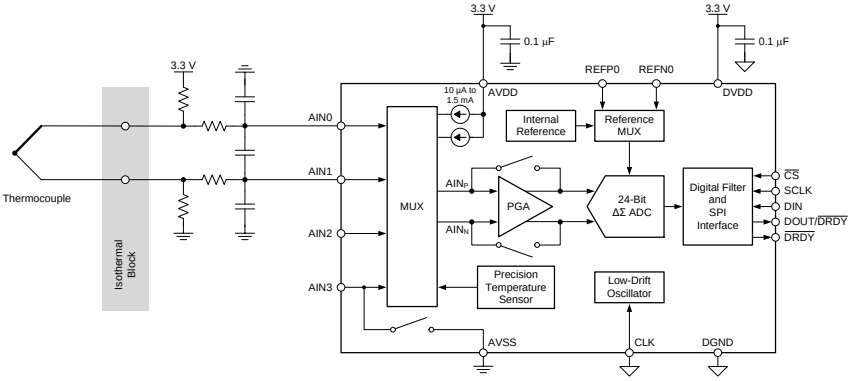


Figure 1

Pin Configuration and Functions

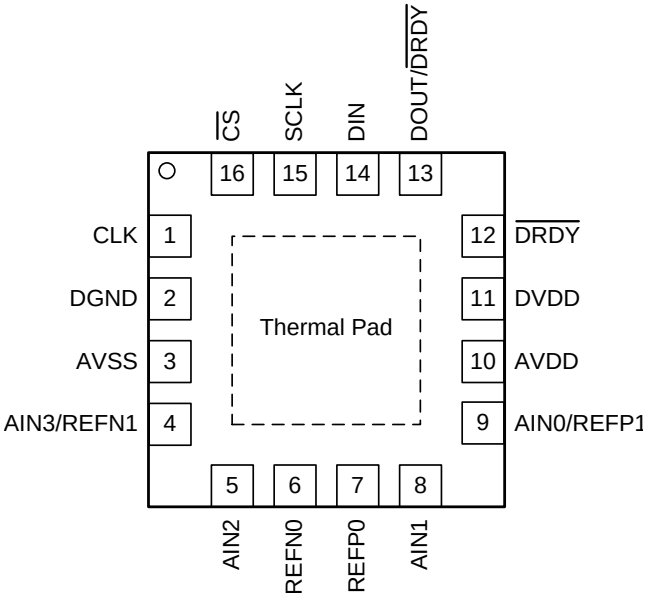


Figure 2.
RVA Package
16-Pin VQFN
Top View

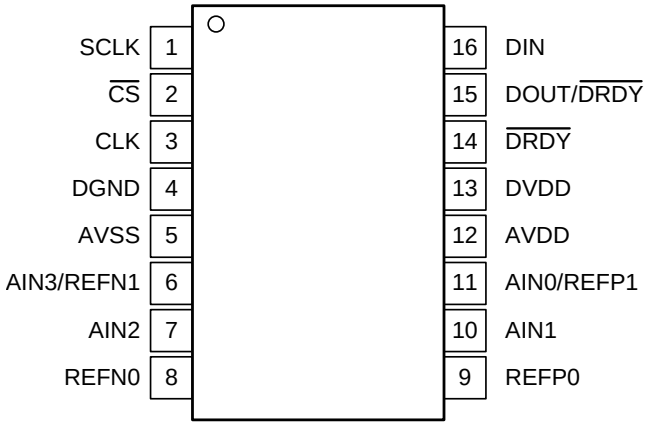


Figure 3
PW Package
16-Pin TSSOP
Top View

Table 2.Pin Functions

PIN			ANALOG OR DIGITAL INPUT/OUTPUT	DESCRIPTION
NAME	NO. RVA	NO. PW		
AIN0/REFP1	9	11	Analog input	Analog input 0, positive reference input 1
AIN1	8	10	Analog input	Analog input 1
AIN2	5	7	Analog input	Analog input 2
AIN3/REFN1	4	6	Analog input	Analog input 3, negative reference input 1. Internal low-side power switch connected between AIN3/REFN1 and AVSS.
AVDD	10	12	Analog	Positive analog power supply
AVSS	3	5	Analog	Negative analog power supply
CLK	1	3	Digital input	External clock source pin. Connect to DGND if not used.
$\overline{CS}$	16	2	Digital input	Chip select; active low. Connect to DGND if not used.
DGND	2	4	Digital	Digital ground
DIN	14	16	Digital input	Serial data input
DOUT/$\overline{DRDY}$	13	15	Digital output	Serial data output combined with data ready; active low
$\overline{DRDY}$	12	14	Digital output	Data ready, active low. Leave unconnected or tie to DVDD using a weak pull-up resistor if not used.
DVDD	11	13	Digital	Positive digital power supply
REFN0	6	8	Analog input	Negative reference input 0
REFP0	7	9	Analog input	Positive reference input 0
SCLK	15	1	Digital input	Serial clock input
Thermal pad		—	—	Thermal power pad. Do not connect or only connect to AVSS.

Specifications

Table 3.Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AVSS	–0.3	7	V
	DVDD to DGND	–0.3	7	V
	AVSS to DGND	–2.8	0.3	V
Analog input voltage	AIN0/REFP1, AIN1, AIN2, AIN3/REFN1, REFP0, REFN0	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	$\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, CLK	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, any pin except power supply pins	–10	10	mA
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 4.ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Table 5.Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Unipolar analog power supply	AVDD to AVSS	2.3		5.5	V
		AVSS to DGND	–0.1	0	0.1	
	Bipolar analog power supply	AVDD to DGND	2.3	2.5	2.75	V
		AVSS to DGND	–2.75	–2.5	–2.3	
	Digital power supply	DVDD to DGND	2.3		5.5	V
ANALOG INPUTS(1)						
V_{IN}	Differential input voltage	$V_{IN} = V_{(AINP)} – V_{(AINN)}$(2)	$–V_{ref}$ / Gain		V_{ref} / Gain	V
$V_{(AINx)}$	Absolute input voltage	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		PGA enabled, gain = 1 to 128	See the *Low-Noise PGA* section			
V_{CM}	Common-mode input voltage	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		PGA enabled, gain = 1 to 128	See the *Low-Noise PGA* section			
VOLTAGE REFERENCE INPUTS(3)						
V_{ref}	Differential reference input voltage	$V_{ref} = V_{(REFPx)} – V_{(REFNx)}$	0.75	2.5	AVDD	V
$V_{(REFNx)}$	Absolute negative reference voltage		AVSS – 0.1		$V_{(REFPx)}$ – 0.75	V
$V_{(REFPx)}$	Absolute positive reference voltage		$V_{(REFNx)}$ + 0.75		AVDD + 0.1	V
EXTERNAL CLOCK SOURCE						
$f_{(CLK)}$	External clock frequency		0.5	4.096	4.5	MHz
	Duty cycle		40%		60%	
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA. AINx denotes one of the four available analog inputs. *PGA disabled* means the low-noise PGA is powered down and bypassed. Gains of 1, 2, and 4 are still possible in this case.
(2) Excluding the effects of offset and gain error. Limited to ±[(AVDD – AVSS) – 0.4 V] / Gain, when the PGA is enabled.
(3) REFPx and REFNx denote one of two available differential reference input pairs.

Table 6.Thermal Information

THERMAL METRIC(1)		MCA1220		UNIT
		VQFN (RVA)	TSSOP (PW)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.4	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.3	35.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.4	44.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.4	43.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

Table 7.Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 3.3 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, DR = 20 SPS, and external V_{ref} = 2.5 V (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current		See the *Typical Characteristics*			
	Differential input current		See the *Typical Characteristics*			
SYSTEM PERFORMANCE						
	Resolution (no missing codes)		24			Bits
DR	Data rate	Normal mode	20, 45, 90, 175, 330, 600, 1000			SPS
		Duty-cycle mode	5, 11.25, 22.5, 44, 82.5, 150, 250			
		Turbo mode	40, 90, 180, 350, 660, 1200, 2000			
	Noise (input-referred)		See the *Noise Performance* section			
INL	Integral nonlinearity	Gain = 1 to 128, V_{CM} = 0.5 AVDD, best fit(2)	–15	±6	15	ppm_{FSR}
V_{IO}	Input offset voltage	PGA disabled, gain = 1 to 4, differential inputs		±4		µV
		Gain = 1, differential inputs, T_A = 25°C	–30	±4	30	
		Gain = 2 to 128, differential inputs		±4		
	Offset drift	PGA disabled, gain = 1 to 4		0.25		µV/°C
		Gain = 1 to 128, T_A = –40°C to +85°C(2)		0.08	0.3	
		Gain = 1 to 128		0.25		
	Offset match	Match between any two inputs		±20		µV
	Gain error	PGA disabled, gain = 1 to 4		±0.015%		
		Gain = 1 to 128, T_A = 25°C	–0.1%	±0.015%	0.1%	
	Gain drift	PGA disabled, gain = 1 to 4		1		ppm/°C
		Gain = 1 to 128(2)		1	4	
NMRR	Normal-mode rejection ratio(2)	50 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 10	105			dB
		60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 11	105			
		50 Hz or 60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 01	90			
CMRR	Common-mode rejection ratio	At dc, gain = 1	90	105		dB
		$f_{(CM)}$ = 50 Hz, DR = 2000 SPS(2)	95	115		
		$f_{(CM)}$ = 60 Hz, DR = 2000 SPS(2)	95	115		
PSRR	Power-supply rejection ratio	AVDD at dc, V_{CM} = 0.5 AVDD, gain = 1	80	105		dB
		DVDD at dc, V_{CM} = 0.5 AVDD, gain = 1(2)	100	115		
INTERNAL VOLTAGE REFERENCE						
	Initial accuracy	T_A = 25°C	2.045	2.048	2.051	V
	Reference drift(2)			5	30	ppm/°C
	Long-term drift	1000 hours		110		ppm
VOLTAGE REFERENCE INPUTS						
	Reference input current	REFP0 = V_{ref}, REFN0 = AVSS		±10		nA
INTERNAL OSCILLATOR						
	Internal oscillator accuracy	Normal mode	–2%	±1%	2%	

(1) *PGA disabled* means the low-noise PGA is powered down and bypassed. Gains of 1, 2, and 4 are still possible in this case.

(2) Minimum and maximum values are ensured by design and characterization data.

Table 7.Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 3.3 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, DR = 20 SPS, and external V_{ref} = 2.5 V (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXCITATION CURRENT SOURCES (IDACs)						
	Current settings			10, 50, 100, 250, 500, 1000, 1500		µA
	Compliance voltage	All current settings			AVDD – 0.9	V
	Accuracy	All current settings, each IDAC	–6%	±1%	6%	
	Current match	Between IDACs (not valid for 10-µA setting)		±0.3%		
	Temperature drift	Each IDAC (not valid for 10-µA setting)		50		ppm/°C
	Temperature drift matching	Between IDACs (not valid for 10-µA setting)		10		ppm/°C
TEMPERATURE SENSOR						
	Conversion resolution			14		Bits
	Temperature resolution			0.03125		°C
	Accuracy	T_A = 0°C to +75°C	–0.5	±0.25	0.5	°C
		T_A = –40°C to +125°C	–1	±0.5	1	
	Accuracy vs analog supply voltage			0.0625	0.25	°C/V
LOW-SIDE POWER SWITCH						
R_{ON}	On-resistance			3.5	5.5	Ω
	Current through switch				30	mA
DIGITAL INPUTS/OUTPUTS						
V_{IH}	High-level input voltage		0.7 DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.3 DVDD	V
V_{OH}	High-level output voltage	I_{OH} = 3 mA	0.8 DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA			0.2 DVDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	–10		10	µA
I_L	Input leakage, low	V_{IL} = DGND	–10		10	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current(3)	Power-down mode		0.1	3	µA
		Normal mode, PGA disabled		240		
		Normal mode, gain = 1 to 16		340	490	
		Normal mode, gain = 32		425		
		Normal mode, gain = 64, 128		510		
I_{DVDD}	Digital supply current(3)	Power-down mode		0.3	5	µA
		Normal mode		75	110	
P_D	Power dissipation(3)	Normal mode, gain = 1 to 16		1.4		mW

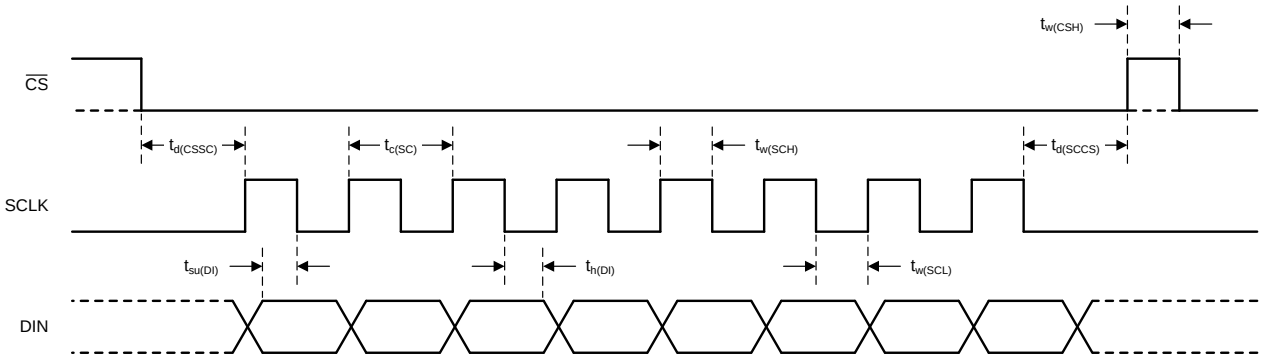
(3) Internal voltage reference selected, internal oscillator enabled, IDACs turned off, and continuous conversion mode. Analog supply current increases by 70 µA, typ (normal mode, turbo mode) when selecting an external reference. Analog supply current increases by 190 µA (typ) when enabling the IDACs (excludes the actual IDAC current).

Table 8.SPI Timing Requirements

over operating ambient temperature range and DVDD = 2.3 V to 5.5 V (unless otherwise noted)

			MIN	MAX	UNIT
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1)		50		ns
$t_{d(SCCS)}$	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge		25		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high		50		ns
$t_{c(SC)}$	SCLK period		150		ns
$t_{w(SCH)}$	Pulse duration, SCLK high		60		ns
$t_{w(SCL)}$	Pulse duration, SCLK low		60		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge		50		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge		25		ns
	SPI timeout(2)	Normal mode, duty-cycle mode		13955	$t_{(MOD)}$

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) See the *SPI Timeout* section for more information.
$t_{(MOD)} = 1 / f_{(MOD)}$. Modulator frequency $f_{(MOD)}$ = 256 kHz (normal mode, duty-cycle mode) and 512 kHz (turbo mode), when using the internal oscillator or an external 4.096-MHz clock.



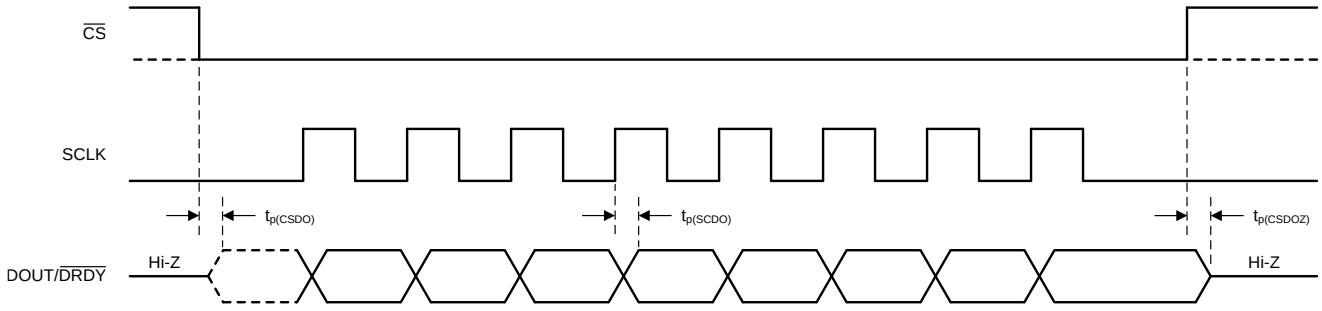
NOTE: Single-byte communication is shown. Actual communication may be multiple bytes.

Figure 4 . Serial Interface Timing Requirements

Table 9.SPI Switching Characteristics

over operating ambient temperature range, DVDD = 2.3 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 10 kΩ to DGND			50	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 10 kΩ to DGND	0		50	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 10 kΩ to DGND			50	ns



NOTE: Single-byte communication is shown. Actual communication may be multiple bytes.

Figure 5. Serial Interface Switching Characteristics

Parameter Measurement Information

Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 1 0 to Table 1 1 summarize the device noise performance.Data are representative of typical noise performance at T_A = 25°C using the internal 2.048-V reference. Data shown are the result of averaging readings from a single device over a time period of approximately 0.75 seconds and are measured with the inputs internally shorted together.

Table 10. Noise in μV_{RMS} (μV_{PP})
at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	5.80	7.32	20.16	31.81	8.69	12.68	23.26	41.20
10	8.13	11.98	21.38	43.61	11.98	13.50	33.62	56.59
20	8.65	16.97	32.36	58.88	14.75	19.38	41.06	73.61
40	18.05	16.64	34.62	45.98	21.12	24.71	33.66	78.75
80	20.67	22.97	36.32	77.75	24.82	33.51	53.60	97.98
160	22.63	30.51	52.00	100.54	35.65	48.68	60.07	160.64
320	23.26	36.52	33.95	57.66	19.86	30.07	59.40	104.13
640	31.10(205.32)	31.92	60.66	92.58	27.66	40.32	82.26	126.47
1000	28.66	34.51	41.42	87.03	28.22	36.28	93.06	185.73
2000	24.56	39.98	53.96	83.71	31.10	49.16	80.19	124.14

Table 11. ENOB from RMS Noise (Noise-Free Bits from Peak-to-Peak Noise)
with PGA Disabled
at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA Enabled)							
	1	2	4	8	16	32	64	128
5	19.4	19.1	17.6	16.9	18.8	18.3	17.4	16.6
10	18.9	18.3	17.5	16.5	18.3	18.2	16.8	16.1
20	18.8	17.8	16.9	16.0	18.0	17.6	16.6	15.7
40	17.8	17.9	16.8	16.4	17.5	17.3	16.8	15.6
80	17.6	17.4	16.7	15.6	17.3	16.8	16.2	15.3
160	17.4	17.0	16.2	15.3	16.8	16.3	16.0	14.6
320	17.4	17.2	16.8	16.1	17.6	17.0	16.0	15.2
640	17.0	16.9	16.0	15.4	17.1	16.6	15.6	14.9
1000	17.1	16.8	16.5	15.5	17.1	16.7	15.4	14.4
2000	17.3	16.6	16.2	15.5	17.0	16.3	15.6	15.0

Feature Description

Multiplexer

The device contains a very flexible input multiplexer, as shown in Figure 6 . Either four single-ended signals, two differential signals, or a combination of two single-ended signals and one differential signal can be measured. The multiplexer is configured by four bits (MUX[3:0]) in the configuration register. When single-ended signals are measured, the negative ADC input (AIN_N) is internally connected to AVSS by a switch within the multiplexer. For system-monitoring purposes, the analog supply (AVDD – AVSS) / 4 or the currently-selected external reference voltage ($V_{(REFPx)} – V_{(REFNx)}$) / 4 can be selected as inputs to the ADC. The multiplexer also offers the possibility to route any of the two programmable current sources to any analog input (AINx) or to any dedicated reference pin (REFP0, REFN0).

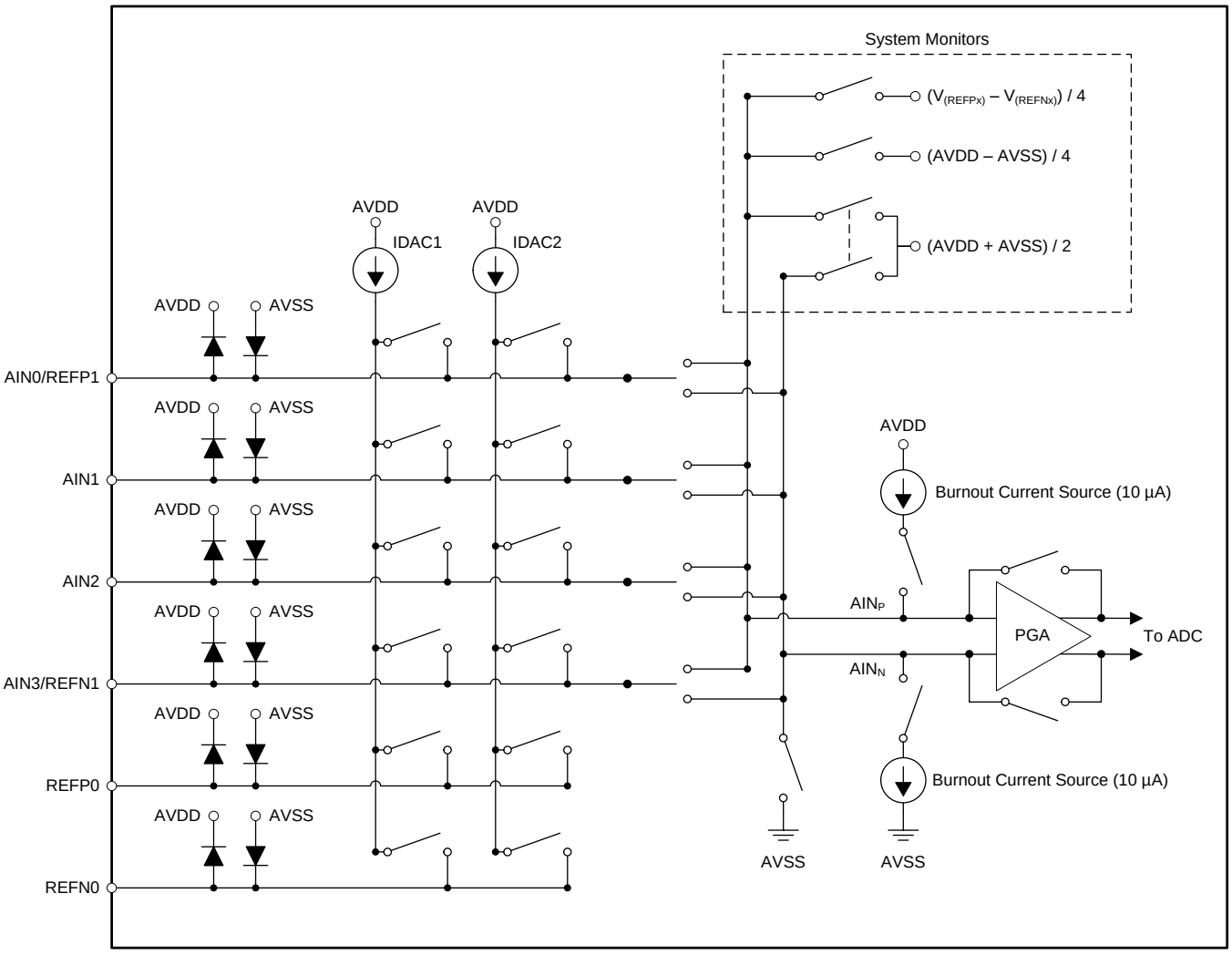


Figure 6 . Analog Input Multiplexer

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by Equation 1 :

$$AVSS – 0.3\ V < V_{(AINx)} < AVDD + 0.3\ V \quad (1)$$

If the voltages on the input pins have any potential to violate these conditions, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unused input on the device may affect conversions taking place on other input pins. If any overdrive on unused inputs is possible, We recommends clamping the signal with external Schottky diodes.

Feature Description (continued)

Low-Noise PGA

The device features a low-noise, low-drift, high input impedance, programmable gain amplifier (PGA). The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Three bits (GAIN[2:0]) in the configuration register are used to configure the gain. A simplified diagram of the PGA is shown in Figure 7 . The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the PGA gain. The PGA input is equipped with an electromagnetic interference (EMI) filter.

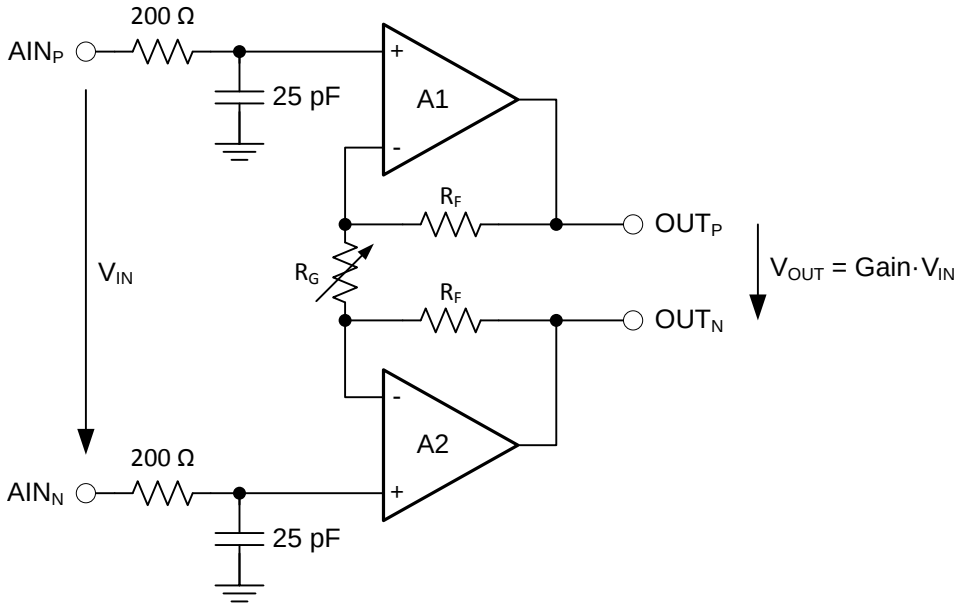


Figure 7 . Simplified PGA Diagram

V_{IN} denotes the differential input voltage $V_{IN} = (V_{(AINP)} - V_{(AINN)})$. The gain of the PGA can be calculated with Equation 2:

$$Gain = 1 + 2 \cdot R_F / R_G \quad (2)$$

Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in Equation 3 :

$$FSR = \pm V_{ref} / Gain \quad (3)$$

Table 1 2 shows the corresponding full-scale ranges when using the internal 2.048-V reference.

Table 1 2 . PGA Full-Scale Range

GAIN SETTING	FSR
1	±2.048 V
2	±1.024 V
4	±0.512 V
8	±0.256 V
16	±0.128 V
32	±0.064 V
64	±0.032 V
128	±0.016 V

PGA Common-Mode Voltage Requirements

To stay within the linear operating range of the PGA, the input signals must meet certain requirements that are discussed in this section.

The outputs of both amplifiers (A1 and A2) in Figure 7 can not swing closer to the supplies (AVSS and AVDD) than 200 mV. If the outputs OUT_P and OUT_N are driven to within 200 mV of the supply rails, the amplifiers saturate and consequently become nonlinear. To prevent this nonlinear operating condition the output voltages must meet Equation 4:

$$AVSS + 0.2\ V \le V_{(OUTN)}, V_{(OUTP)} \le AVDD - 0.2\ V \quad (4)$$

Translating the requirements of Equation 4 into requirements referred to the PGA inputs (AIN_P and AIN_N) is beneficial because there is no direct access to the outputs of the PGA. The PGA employs a symmetrical design, therefore the common-mode voltage at the output of the PGA can be assumed to be the same as the common-mode voltage of the input signal, as shown in Figure 8 .

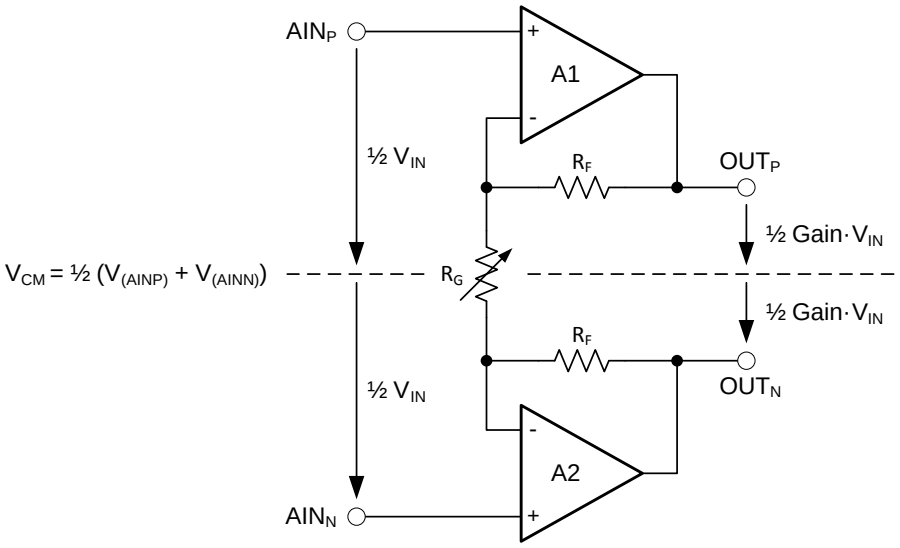


Figure 8 . PGA Common-Mode Voltage

The common-mode voltage is calculated using Equation 5 :

$$V_{CM} = ½\ (V_{(AINP)} + V_{(AINN)}) = ½\ (V_{(OUTP)} + V_{(OUTN)}) \quad (5)$$

The voltages at the PGA inputs (AIN_P and AIN_N) can be expressed as Equation 6 and Equation 7 :

$$V_{(AINP)} = V_{CM} + ½\ V_{IN} \quad (6)$$

$$V_{(AINN)} = V_{CM} - ½\ V_{IN} \quad (7)$$

The output voltages ($V_{(OUTP)}$ and $V_{(OUTN)}$) can then be calculated as Equation 8 and Equation 9 :

$$V_{(OUTP)} = V_{CM} + ½\ Gain \cdot V_{IN} \quad (8)$$

$$V_{(OUTN)} = V_{CM} - ½\ Gain \cdot V_{IN} \quad (9)$$

The requirements for the output voltages of amplifiers A1 and A2 (Equation 7) can now be translated into requirements for the input common-mode voltage range using Equation 8 and Equation 9 , which are given in Equation 10 and Equation 11:

$$V_{CM\ (MIN)} \ge AVSS + 0.2\ V + ½\ Gain \cdot V_{IN\ (MAX)} \quad (10)$$

$$V_{CM\ (MAX)} \le AVDD - 0.2\ V - ½\ Gain \cdot V_{IN\ (MAX)} \quad (11)$$

In order to calculate the minimum and maximum common-mode voltage limits, the maximum differential input voltage ($V_{IN\ (MAX)}$) that occurs in the application must be used. $V_{IN\ (MAX)}$ can be less than the maximum possible FS value.

In addition to Equation 10, the minimum V_{CM} must also meet Equation 12 because of the specific design implementation of the PGA.

$$V_{CM\ (MIN)} \ge AVSS + ¼\ (AVDD - AVSS) \quad (12)$$

Figure 9 and Figure 10 show a graphical representation of the common-mode voltage limits for AVDD = 3.3 V and AVSS = 0 V, with gain = 1 and gain = 16, respectively.

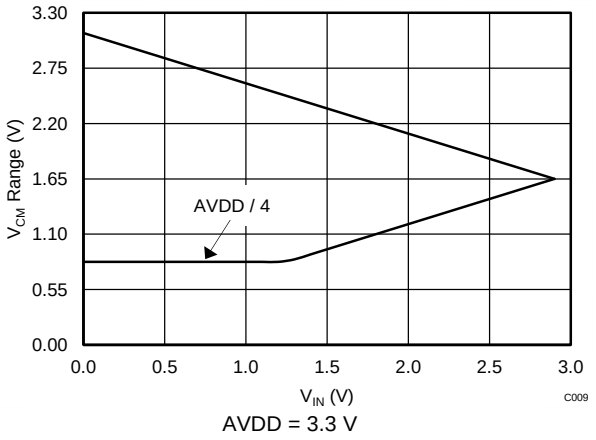


Figure 9 . Common-Mode Voltage Limits (Gain = 1)

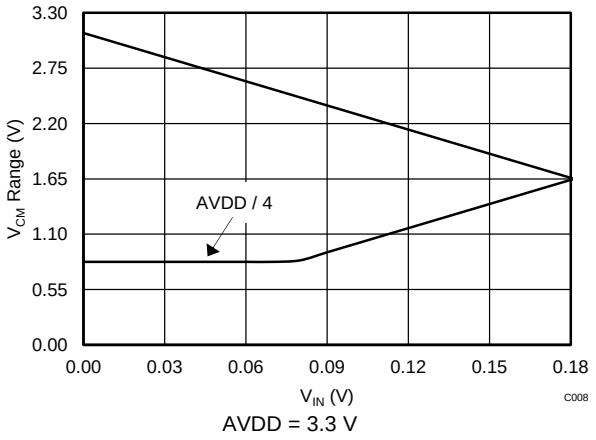


Figure 10. Common-Mode Voltage Limits (Gain = 16)

The following discussion explains how to apply Equation 13 through Equation 15 to a hypothetical application. The setup for this example is AVDD = 3.3 V, AVSS = 0 V, and gain = 16, using an external reference, V_{ref} = 2.5 V. The maximum possible differential input voltage V_{IN} = ($V_{(AINP)}$ – $V_{(AINN)}$) that can be applied is then limited to the full-scale range of FSR = ±2.5 V / 16 = ±0.156 V. Consequently, Equation 13 through Equation 15 yield an allowed V_{CM} range of 1.45 V ≤ V_{CM} ≤ 1.85 V.

If the sensor signal connected to the inputs in this hypothetical application does not make use of the entire full-scale range but is limited to $V_{IN\ (MAX)}$ = ±0.1 V, for example, then this reduced input signal amplitude relaxes the V_{CM} restriction to 1.0 V ≤ V_{CM} ≤ 2.3 V.

In the case of a fully-differential sensor signal, each input (AIN_P, AIN_N) can swing up to ±50 mV around the common-mode voltage ($V_{(AINP)}$ + $V_{(AINN)}$) / 2, which must remain between the limits of 1.0 V and 2.3 V. The output of a symmetrical wheatstone bridge is an example of a fully-differential signal. Figure 12 shows a situation where the common-mode voltage of the input signal is at the lowest limit. $V_{(OUTN)}$ is exactly at 0.2 V in this case. Any further decrease in common-mode voltage (V_{CM}) or increase in differential input voltage (V_{IN}) drives $V_{(OUTN)}$ below 0.2 V and saturates amplifier A2.

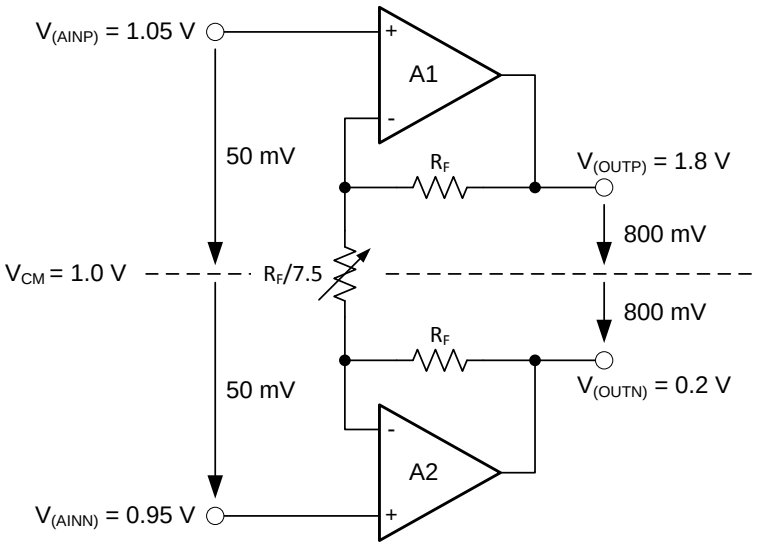


Figure 1 1 . Example where V_{CM} is at Lowest Limit

In contrast, the signal of an RTD is of a pseudo-differential nature (if implemented as shown in the *RTD Measurement* section), where the negative input is held at a constant voltage other than 0 V and only the voltage on the positive input changes. When a pseudo-differential signal must be measured, the negative input in this example must be biased at a voltage between 0.95 V and 2.25 V. The positive input can then swing up to $V_{IN\ (MAX)}$ = 100 mV above the negative input. Note that in this case the common-mode voltage changes at the same time the voltage on the positive input changes. That is, while the input signal swings between 0 V ≤ V_{IN} ≤ $V_{IN\ (MAX)}$, the common-mode voltage swings between $V_{(AINN)}$ ≤ V_{CM} ≤ $V_{(AINN)}$ + ½ $V_{IN\ (MAX)}$. Satisfying the common-mode voltage requirements for the maximum input voltage $V_{IN\ (MAX)}$ ensures the requirements are met throughout the entire signal range.

Figure 12 and Figure 13show examples of both fully-differential and pseudo-differential signals, respectively.

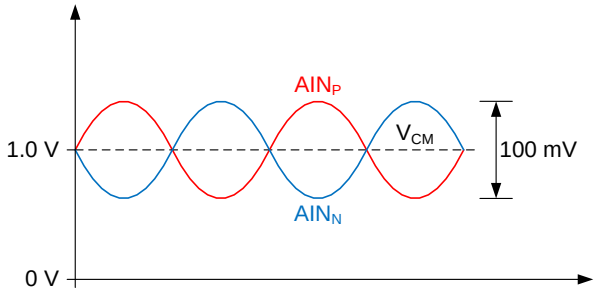


Figure 1 2 . Fully-Differential Input Signal

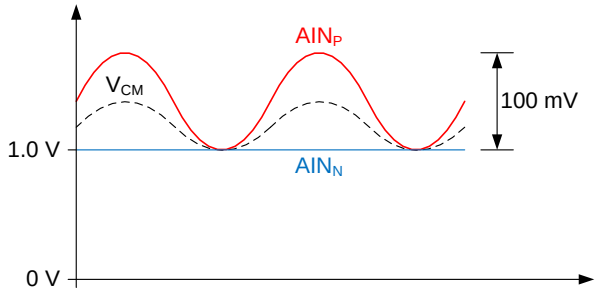


Figure 13. Pseudo-Differential Input Signal

NOTE

Remember, common-mode voltage requirements with PGA enabled (Equation 13 to Equation 15) are as follows:

- $V_{CM\ (MIN)}$ ≥ AVSS + ¼ (AVDD – AVSS)
- $V_{CM\ (MIN)}$ ≥ AVSS + 0.2 V + ½ Gain · $V_{IN\ (MAX)}$
- $V_{CM\ (MAX)}$ ≤ AVDD – 0.2 V – ½ Gain · $V_{IN\ (MAX)}$

Bypassing the PGA

At gains of 1, 2, and 4, the device can be configured to disable and bypass the low-noise PGA by setting the PGA_BYPASS bit in the configuration register. Disabling the PGA lowers the overall power consumption and also removes the restrictions of Equation 13 through Equation 15 for the common-mode input voltage range, V_{CM}. The usable absolute and common-mode input voltage range is (AVSS – 0.1 V ≤ $V_{(AINx)}$, V_{CM} ≤ AVDD + 0.1 V) when the PGA is disabled.

In order to measure single-ended signals that are referenced to AVSS (AIN_P = V_{IN}, AIN_N = AVSS), the PGA must be bypassed. Configure the device for single-ended measurements by either connecting one of the analog inputs to AVSS externally or by using the internal AVSS connection of the multiplexer (MUX[3:0] settings 1000 through 1011). When configuring the internal multiplexer for settings where AIN_N = AVSS (MUX[3:0] = 1000 through 1011) the PGA is automatically bypassed and disabled irrespective of the PGA_BYPASS setting and gain is limited to 1, 2, and 4. In case gain is set to greater than 4, the device limits gain to 4.

When the PGA is disabled, the device uses a buffered switched-capacitor stage to obtain gains of 1, 2, and 4. An internal buffer in front of the switched-capacitor stage ensures that the effect on the input loading resulting from the capacitor charging and discharging is minimal.
For signal sources with high output impedance, external buffering may still be necessary. Note that active buffers introduce noise and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

Modulator

A ΔΣ modulator is used in the MCA1220 to convert the analog input voltage into a pulse code modulated (PCM)data stream. The modulator runs at a modulator clock frequency of $f_{(MOD)} = f_{(CLK)} / 16$ in normal and duty-cycle mode and $f_{(MOD)} = f_{(CLK)} / 8$ in turbo mode, where $f_{(CLK)}$is either provided by the internal oscillator or the ext ernal clock source. Table 10 shows the modulator frequency for each operating mode using either the int ernal oscillator or an external clock of 4.096 MHz.

A third-order Δ-Σ modulator is used in the device. The modulator converts the analog input voltage into a pulse density modulation (PDM) data stream. To save power, the modulator clock operates in the range of 32kHz to 512kHz, supporting different data rates as shown in Table 13.

Table 13. Modulator Clock Frequency for Different Operating Modes(1)

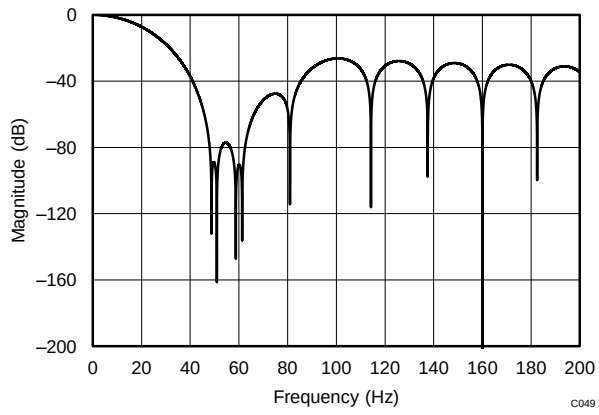
DATA RATE(SPS)	MODULATOR RATE $f_{(MOD)}$(SPS)	f_{CLK}/f_{MOD}
5,10,20	32	128
40,80,160	128	32
320,640,1000	256	16
2000	512	8

(1) Using the internal oscillator or an external 4.096-MHz clock.

Digital Filter

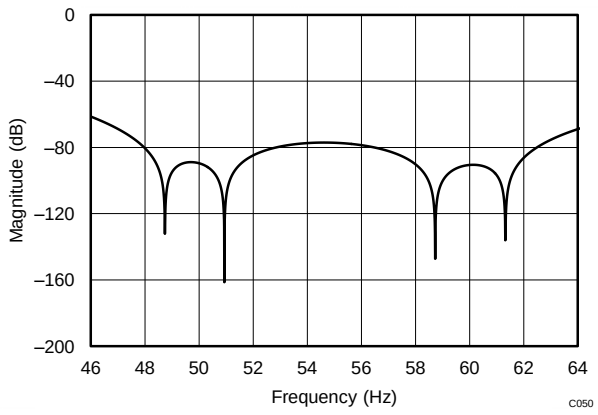
The device uses a linear-phase finite impulse response (FIR) digital filter that performs both filtering and decimation of the digital data stream coming from the modulator. The digital filter is automatically adjusted for the different data rates and always settles within a single cycle. At data rates of 5 SPS and 20 SPS, the filter can be configured to reject 50-Hz or 60-Hz line frequencies or to simultaneously reject 50 Hz and 60 Hz. Two bits (50/60[1:0]) in the configuration register are used to configure the filter accordingly. The frequency responses of the digital filter are illustrated in Figure 14 to Figure 2 7 for different output data rates using the internal oscillator or an external 4.096-MHz clock.

The filter notches and output data rate scale proportionally with the clock frequency. For example, a notch that appears at 20 Hz when using a 4.096-MHz clock appears at 10 Hz if a 2.048-MHz clock is used. Note that the internal oscillator can vary over temperature as specified in the *Electrical Characteristics* table. The data rate or conversion time, respectively, and filter notches consequently vary by the same amount. Consider using an external precision clock source if a digital filter notch at a specific frequency with a tighter tolerance is required.



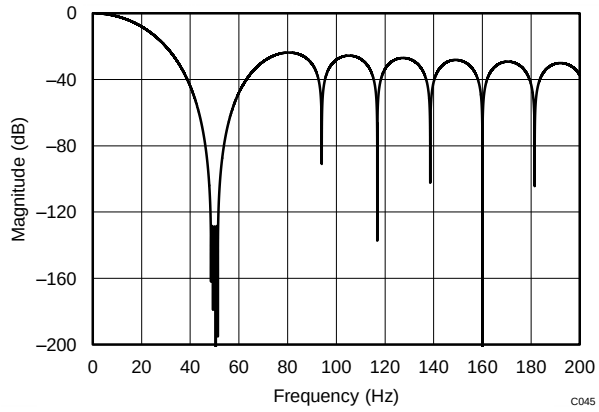
Simultaneous 50-Hz and 60-Hz Rejection, 50/60[1:0] = 01

Figure 1 4 . Filter Response (DR = 20 SPS)



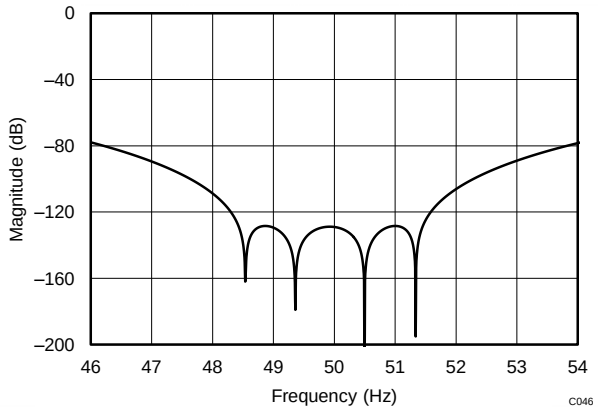
Simultaneous 50-Hz and 60-Hz Rejection, 50/60[1:0] = 01

Figure 15. Detailed View of Filter Response (DR = 20 SPS)



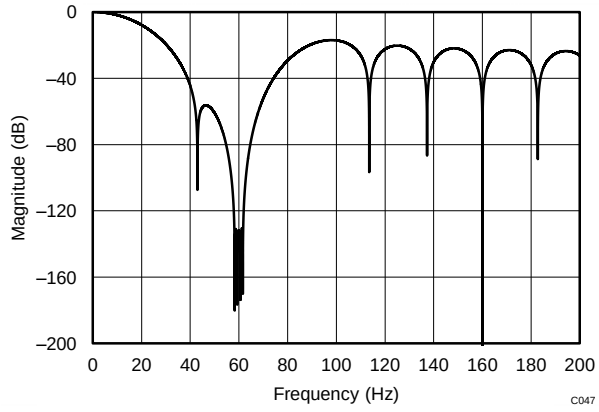
50-Hz Rejection Only, 50/60[1:0] = 10

Figure 16. Filter Response (DR = 20 SPS)



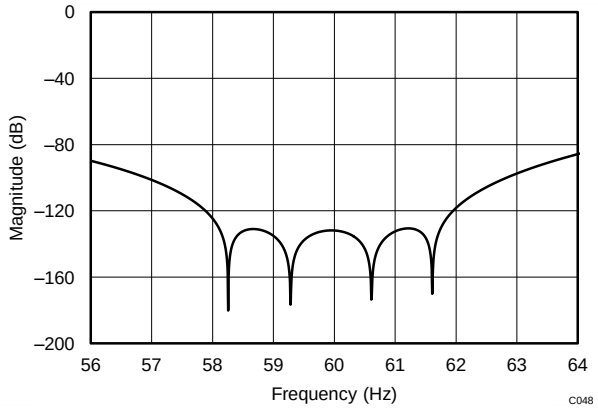
50-Hz Rejection Only, 50/60[1:0] = 10

Figure 17. Detailed View of Filter Response (DR = 20 SPS)



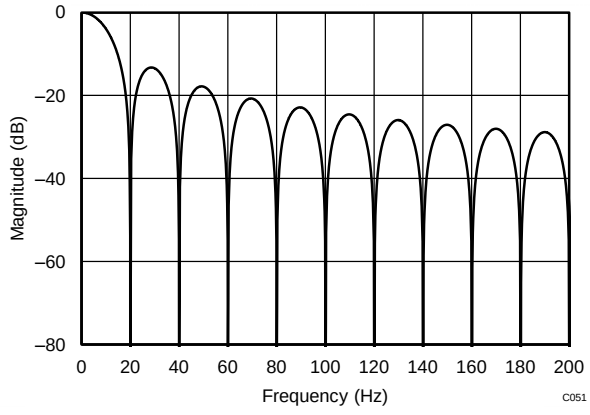
60-Hz Rejection Only, 50/60[1:0] = 11

Figure 18. Filter Response (DR = 20 SPS)



60-Hz Rejection Only, 50/60[1:0] = 11

Figure 1 9 . Detailed View of Filter Response (DR = 20 SPS)



50/60[1:0] = 00

Figure 20. Filter Response (DR = 20 SPS)

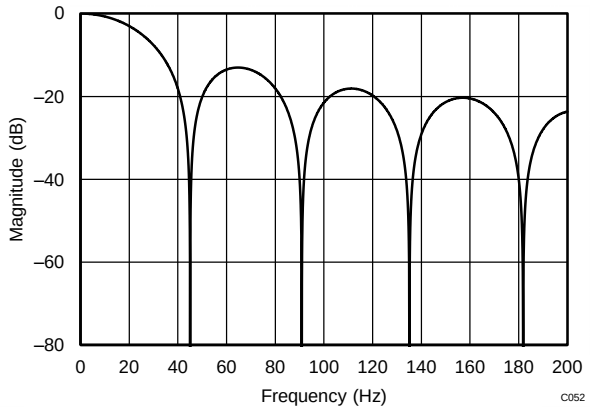


Figure 21. Filter Response (DR = 45 SPS)

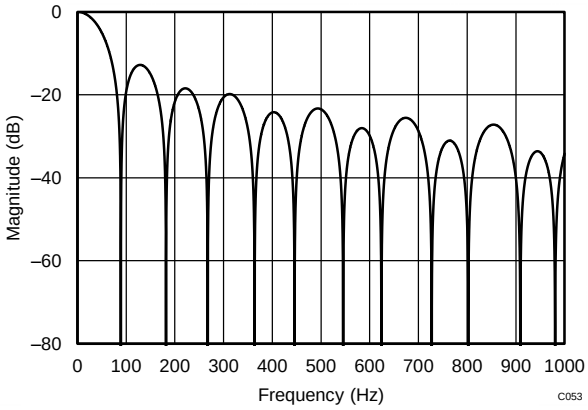


Figure 22. Filter Response (DR = 90 SPS)

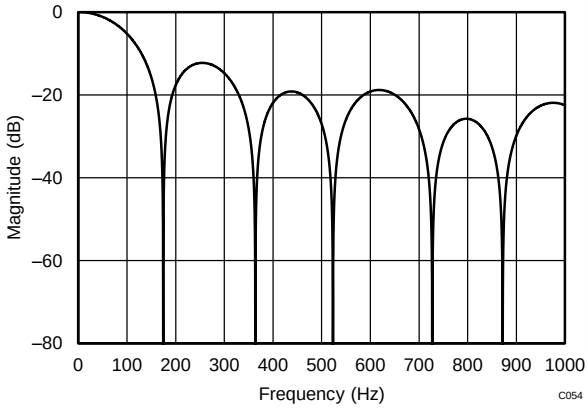


Figure 23. Filter Response (DR = 175 SPS)

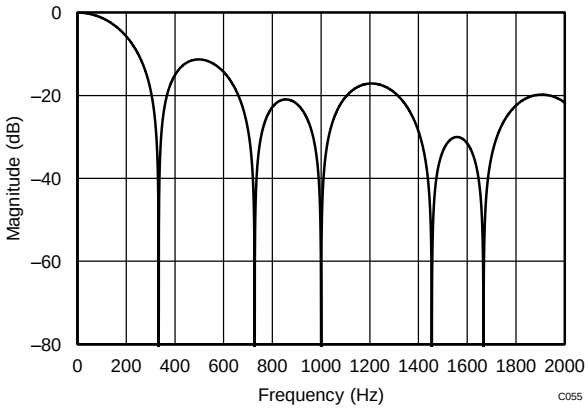


Figure 24. Filter Response (DR = 330 SPS)

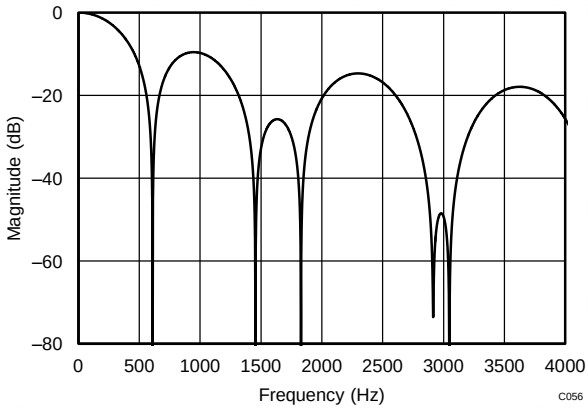


Figure 25. Filter Response (DR = 600 SPS)

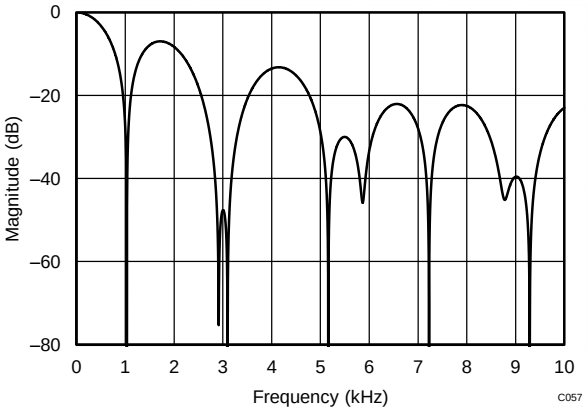


Figure 26. Filter Response (DR = 1 kSPS)

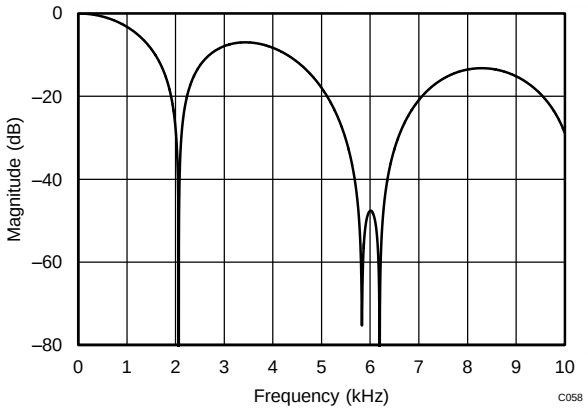


Figure 27. Filter Response (DR = 2 kSPS)

Output Data Rate

Table 14shows the actual conversion times for each data rate setting. The values provided are in terms of $t_{(CLK)}$ cycles using an external clock with a clock frequency of $f_{(CLK)}$ = 4.096 MHz. The data rates scale proportionally in case an external clock with a frequency other than 4.096 MHz is used.

Continuous conversion mode data rates are timed from one $\overline{DRDY}$ falling edge to the next $\overline{DRDY}$ falling edge. The first conversion starts 210 · $t_{(CLK)}$ (normal mode, duty-cycle mode) or 114 · $t_{(CLK)}$ (turbo mode) after the last SCLK falling edge of the START/SYNC command.

Single-shot mode data rates are timed from the last SCLK falling edge of the START/SYNC command to the $\overline{DRDY}$ falling edge and rounded to the next $t_{(CLK)}$. In case the internal oscillator is used, an additional oscillator wake-up time of up to 50 µs (normal mode, duty-cycle mode) or 25 µs (turbo mode) must be added in single-shot mode. The internal oscillator starts to power up at the first SCLK rising edge of the START/SYNC command. If an SCLK frequency higher than 160 kHz (normal mode, duty-cycle mode) or 320 kHz (turbo mode) is used, the oscillator may not be fully powered up at the end of the START/SYNC command. The ADC then waits until the internal oscillator is fully powered up before starting a conversion.

Single-shot conversion times in duty-cycle mode are the same as in normal mode. See the *Duty-Cycle Mode* section for more details on duty-cycle mode operation.

Table 14. Conversion Times

NOMINAL DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	ACTUAL CONVERSION TIME ($t_{(CLK)}$)	
		CONTINUOUS CONVERSION MODE	SINGLE-SHOT MODE
NORMAL MODE			
20	13.1	204768	204850
45	20.0	91120	91218
90	39.6	46128	46226
175	77.8	23664	23762
330	150.1	12464	12562
600	279.0	6896	6994
1000	483.8	4144	4242
DUTY-CYCLE MODE			
5	13.1	823120	n/a
11.25	20.0	364560	n/a
22.5	39.6	184592	n/a
44	77.8	94736	n/a
82.5	150.1	49936	n/a
150	279.0	27664	n/a
250	483.8	16656	n/a
TURBO MODE			
40	26.2	102384	102434
90	39.9	45560	45618
180	79.2	23064	23122
350	155.6	11832	11890
660	300.3	6232	6290
1200	558.1	3448	3506
2000	967.6	2072	2130

Note that even though the conversion time at the 20-SPS setting is not exactly 1 / 20 Hz = 50 ms, this discrepancy does not affect the 50-Hz or 60-Hz rejection. To achieve the 50-Hz and 60-Hz rejection specified in the *Electrical Characteristics* table, the external clock frequency must be 4.096 MHz. When using the internal oscillator, the conversion time and filter notches vary by the amount specified in the *Electrical Characteristics* table for oscillator accuracy.

Voltage Reference

The device offers an integrated low-drift, 2.048-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the device offers two differential reference input pairs (REFP0, REFN0 and REFP1, REFN1). In addition, the analog supply (AVDD) can be used as a reference.

The reference source is selected by two bits (VREF[1:0]) in the configuration register. By default, the internal reference is selected. The internal voltage reference requires less than 25 µs to fully settle after power-up, when coming out of power-down mode, or when switching from an external reference source to the internal reference.

The differential reference inputs allow freedom in the reference common-mode voltage. REFP0 and REFN0 are dedicated reference inputs whereas REFP1 and REFN1 are shared with inputs AIN0 and AIN3, respectively. All reference inputs are internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference. When used in ratiometric applications, the reference inputs do not load the external circuitry. Note that the analog supply current increases when using an external reference because the reference buffers are enabled.

In most cases the conversion result is directly proportional to the stability of the reference source. Any noise and drift of the voltage reference is reflected in the conversion result.

Clock Source

The device system clock can either be provided by the internal low-drift oscillator or by an external clock source on the CLK input. Connect the CLK pin to DGND before power-up or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator after two rising edges on the CLK pin are detected. The device then operates on the external clock. After the ADS1220 switches to the external clock, the device can only be switched back to the internal oscillator by cycling the power supplies or by sending a RESET command.

Excitation Current Sources

The device provides two matched programmable excitation current sources (IDACs) for RTD applications. The output current of the current sources can be programmed to 10 µA, 50 µA, 100 µA, 250 µA, 500 µA, 1000 µA, or 1500 µA using the respective bits (IDAC[2:0]) in the configuration register. Each current source can be connected to any of the analog inputs (AINx) as well as to any of the dedicated reference inputs (REFP0 and REFN0). Both current sources can also be connected to the same pin. Routing of the IDACs is configured by bits (I1MUX[2:0], I2MUX[2:0]) in the configuration register. Care must be taken not to exceed the compliance voltage of the IDACs. In other words, limit the voltage on the pin where the IDAC is routed to ≤ (AVDD – 0.9 V), otherwise the specified accuracy of the IDAC current is not met. For three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *3-Wire RTD Measurement* section for more details).

The IDACs require up to 200 µs to start up after the IDAC current is programmed to the respective value using bits IDAC[2:0]. If configuration registers 2 and 3 are not written during the same WREG command,We recommends to first set the IDAC current to the respective value using bits IDAC[2:0 and thereafter select the routing for each IDAC (I1MUX[2:0], I2MUX[2:0]).

In single-shot mode, the IDACs remain active between any two conversions if the IDAC[2:0] bits are set to a value other than 000. However, the IDACs are powered down whenever the POWERDOWN command is issued.

Note that the analog supply current increases when enabling the IDACs (that is, when the IDAC[2:0] bits are set to a value other than 000). The IDAC circuit needs this bias current to operate even when the IDACs are not routed to any pin (I1MUX[2:0] = I2MUX[2:0] = 000). In addition, the selected output current is drawn from the analog supply when I1MUX[2:0] or I2MUX[2:0] are set to a value other than 000.

Low-Side Power Switch

A low-side power switch with low on-resistance connected between the analog input AIN3/REFN1 and AVSS is integrated in the device as well. This power switch can be used to reduce system power consumption in bridge sensor applications by powering down the bridge circuit between conversions. When the respective bit (PSW) in the configuration register is set, the switch automatically closes when the START/SYNC command is sent and opens when the POWERDOWN command is issued. Note that the switch stays closed between conversions in single-shot mode in case the PSW bit is set to 1. The switch can be opened at any time by setting the PSW bit to 0. By default, the switch is always open.

Sensor Detection

To help detect a possible sensor malfunction, the device provides internal 10-µA, burn-out current sources. When enabled by setting the respective bit (BCS) in the configuration register, one current source sources current to the positive analog input (AIN_P) currently selected while the other current source sinks current form the selected negative analog input (AIN_N).

In case of an open circuit in the sensor, these burn-out current sources pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading may also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading may indicate a shorted sensor. Note that the absolute value of the burn-out current sources typically varies by ±10% and the internal multiplexer adds a small series resistance. Therefore, distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. In other words, even if the sensor is shorted, the voltage drop across the external filter resistance and the residual resistance of the multiplexer causes the output to read a value higher than zero.

Keep in mind that ADC readings of a functional sensor may be corrupted when the burn-out current sources are enabled. We recommends disabling the burnout current sources when preforming the precision measurement ,and only enabling them to test for sensor fault conditions.

System Monitor

The device provides some means for monitoring the analog power supply and the external voltage reference. To select a monitoring voltage, the internal multiplexer (MUX[3:0]) must be configured accordingly in the configuration register. The device automatically bypasses the PGA and sets the gain to 1, irrespective of the configuration register settings while the monitoring feature is used. Note that the system monitor function only provides a coarse result and is not meant to be a precision measurement.

When measuring the analog power supply (MUX[3:0] = 1101), the resulting conversion is approximately (AVDD – AVSS) / 4. The device uses the internal 2.048-V reference for the measurement regardless of what reference source is selected in the configuration register (VREF[1:0]).

When monitoring one of the two possible external reference voltage sources (MUX[3:0] = 1100), the result is approximately ($V_{(REFPx)} – V_{(REFNx)}$) / 4. REFPx and REFNx denote the external reference input pair selected in the configuration register (VREF[1:0]). The device automatically uses the internal reference for the measurement.

Offset Calibration

The internal multiplexer offers the option to short both PGA inputs (AIN_P and AIN_N) to mid-supply (AVDD + AVSS) / 2. This option can be used to measure and calibrate the device offset voltage by storing the result of the shorted input voltage reading in a microcontroller and consequently subtracting the result from each following reading. TI recommends taking multiple readings with the inputs shorted and averaging the result to reduce the effect of noise.

Temperature Sensor

The MCA1220 offers an integrated precision temperature sensor. The temperature sensor mode is enabled by setting bit TS = 1 in the configuration register. When in temperature sensor mode, the settings of configuration register 0 have no effect and the device uses the internal reference for measurement, regardless of the selected voltage reference source. Temperature readings follow the same process as the analog inputs for starting and reading conversion results. Temperature data are represented as a 14-bit result that is left-justified within the 24-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the three data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format, as shown in Table 15.

Table 15. 14-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–40	11 1011 0000 0000	3B00

Device Functional Modes

Power-Up and Reset

When the device powers up, a reset is performed. The reset process takes approximately 50 µs. After this power-up reset time, all internal circuitry (including the voltage reference) are stable and communication with the device is possible. As part of the reset process, the device sets all bits in the configuration registers to the respective default settings. By default, the device is set to single-shot mode. After power-up, the device performs a single conversion using the default register settings and then enters a low-power state. When the conversion is complete, the $\overline{\text{DRDY}}$ pin transitions from high to low. The high-to-low transition of the $\overline{\text{DRDY}}$ pin can be used to signal that the ADS1220 is operational and ready to use. The power-up behavior is intended to prevent systems with tight power-supply requirements from encountering a current surge during power-up.

Conversion Modes

The device can be operated in one of two conversion modes that can be selected by the CM bit in the configuration register. These conversion modes are single-shot and continuous conversion mode.

Single-Shot Mode

In single-shot mode, the device only performs a conversion when a START/SYNC command is issued. The device consequently performs one single conversion and returns to a low-power state afterwards. The internal oscillator and all analog circuitry (except for the excitation current sources) are turned off while the device waits in this low-power state until the next conversion is started. In addition, every write access to any configuration register also starts a new conversion. Writing to any configuration register while a conversion is ongoing functions as a new START/SYNC command that stops the current conversion and restarts a single new conversion. Each conversion is fully settled (assuming the analog input signal settles to its final value before the conversion starts) because the device digital filter settles within a single cycle.

Continuous Conversion Mode

In continuous conversion mode, the device continuously performs conversions. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion.

In order to start continuous conversion mode, the CM bit must be set to 1 followed by a START/SYNC command. The first conversion starts $210 \cdot t_{(CLK)}$ (normal mode, duty-cycle mode) or $114 \cdot t_{(CLK)}$ (turbo mode) after the last SCLK falling edge of the START/SYNC command. Writing to any configuration register during an ongoing conversion restarts the current conversion.We recommends always sending a START/SYNC command immediately after the CM bit is set to 1.

Device Functional Modes (continued)

Operating Modes

In addition to the different conversion modes, the device can also be operated in different operating modes that can be selected to trade-off power consumption, noise performance, and output data rate. These modes are: normal mode, duty-cycle mode, turbo mode, and power-down mode.

Normal Mode

Normal mode is the default mode of operation after power-up. In this mode, the internal modulator of the ΔΣ ADC runs at a modulator clock frequency of $f_{(MOD)} = f_{(CLK)} / 16$, where the system clock ($f_{(CLK)}$) is either provided by the internal oscillator or the external clock source. The modulator frequency is 256 kHz when using the internal oscillator. Normal mode offers output data rate options ranging from 20 SPS to 1 kSPS with the internal oscillator. The data rate is selected by the DR[2:0] bits in the configuration register. In case an external clock source with a clock frequency other than 4.096 MHz is used, the data rates scale accordingly. For example, using an external clock with $f_{(CLK)}$ = 2.048 MHz yields data rates ranging from 10 SPS to 500 SPS.

Duty-Cycle Mode

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the device supports an automatic duty-cycle mode that can yield significant power savings by periodically entering a low-power state between conversions. In principle, the device runs in normal mode with a duty cycle of 25%. This functionality means the device performs one conversion in the same manner as when running in normal mode but then automatically enters a low power-state for three consecutive conversion cycles. The noise performance in duty-cycle mode is therefore comparable to the noise performance in normal mode at four times the data rate. Data rates in duty-cycle mode range from 5 SPS to 250 SPS with the internal oscillator.

Turbo Mode

Applications that require higher data rates up to 2 kSPS can operate the device in turbo mode. In this mode, the internal modulator runs at a higher frequency of $f_{(MOD)} = f_{(CLK)} / 8$. $f_{(MOD)}$ equals 512 kHz when the internal oscillator or an external 4.096-MHz clock is used. Note that the device power consumption increases because the modulator runs at a higher frequency.Running the MCA1220 in turbo mode at a comparable output data rate as in normal mode yields better noise performance. For example, the input-referred noise at 90 SPS in turbo mode is lower than the input-referred noise at 90 SPS in normal mode.

Power-Down Mode

When the POWERDOWN command is issued, the device enters power-down mode after completing the current conversion. In this mode, all analog circuitry (including the voltage reference and both IDACs) are powered down, the low-side power switch is opened, and the device typically only uses 400 nA of current. While in power-down mode, the device holds the configuration register settings and responds to commands, but does not perform any data conversions.

Issuing a START/SYNC command wakes up the device and either starts a single conversion or starts continuous conversion mode, depending on the conversion mode selected by the CM bit. Note that writing to any configuration register wakes up the device as well, but only starts a single conversion regardless of the selected conversion mode (CM).

Programming

Data Format

The device provides 24 bits of data in binary twos complement format. The size of one code (LSB) is calculated using Equation 16.

$$1\ \text{LSB} = (2 \cdot V_{ref} / \text{Gain}) / 2^{24} = +\text{FS} / 2^{23} \quad (16)$$

A positive full-scale input [$V_{IN} \geq (+\text{FS} - 1\ \text{LSB}) = (V_{ref} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{ref} / \text{Gain}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

Table 16 summarizes the ideal output codes for different input signals.

Table 16. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} ($AIN_P - AIN_N$)	IDEAL OUTPUT CODE(1)
$\geq \text{FS}\ (2^{23} - 1) / 2^{23}$	7FFFFFh
$\text{FS} / 2^{23}$	000001h
0	000000h
$-\text{FS} / 2^{23}$	FFFFFFh
$\leq -\text{FS}$	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

Mapping of the analog input signal to the output codes is shown in Figure 29.

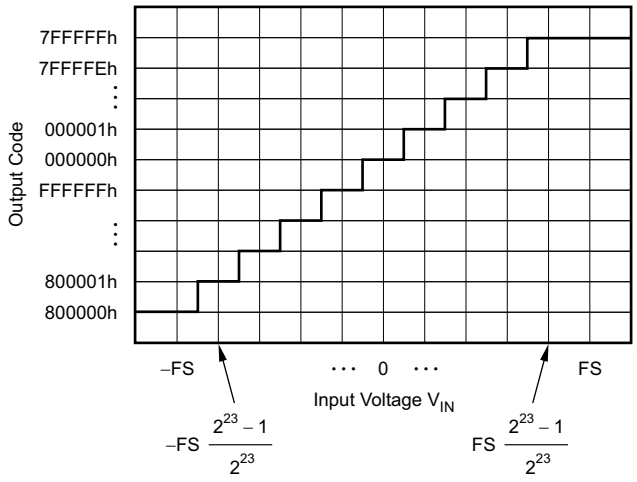


Figure 28. Code Transition Diagram

Commands

The device offers six different commands to control device operation, as shown in Table 17. Four commands are stand-alone instructions (RESET, START/SYNC, POWERDOWN, and RDATA). The commands to read (RREG) and write (WREG) configuration register data from and to the device require additional information as part of the instruction.

Table 17. Command Definitions

COMMAND	DESCRIPTION	COMMAND BYTE (1)
RESET	Reset the device	0000 011x
START/SYNC	Start or restart conversions	0000 100x
POWERDOWN	Enter power-down mode	0000 001x
RDATA	Read data by command	0001 xxxx
RREG	Read *nn* registers starting at address *rr*	0010 *rrnn*
WREG	Write *nn* registers starting at address *rr*	0100 *rrnn*

(1) Operands: rr = configuration register (00 to 11), nn = number of bytes – 1 (00 to 11), and x = don't care.

Application and Implementation

Serial Interface Connections

The principle serial interface connections for the ADS1220 are shown in Figure 2 9 .

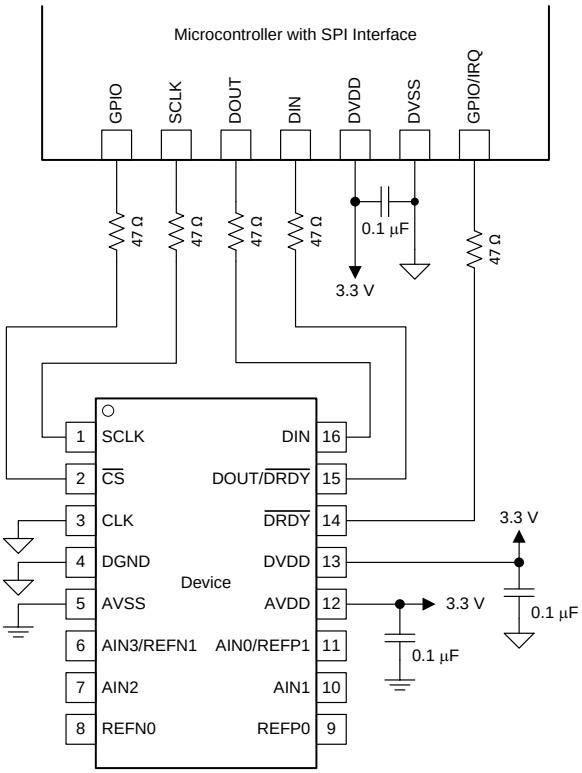


Figure 2 9 . Serial Interface Connections

Most microcontroller SPI peripherals can operate with the MCA1220. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the device can be found in the *SPI Timing Requirements* section.

We recommends placing 47-Ω resistors in series with all digital input and output pins ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and DRDY). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

Application Information (continued)

Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components are folded back and show up in the actual frequency band of interest below half the sampling frequency. Note that inside a ΔΣ ADC, the input signal is sampled at the modulator frequency $f_{(MOD)}$ and not at the output data rate. The filter response of the digital filter repeats at multiples of the sampling frequency ($f_{(MOD)}$), as shown in Figure 30. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

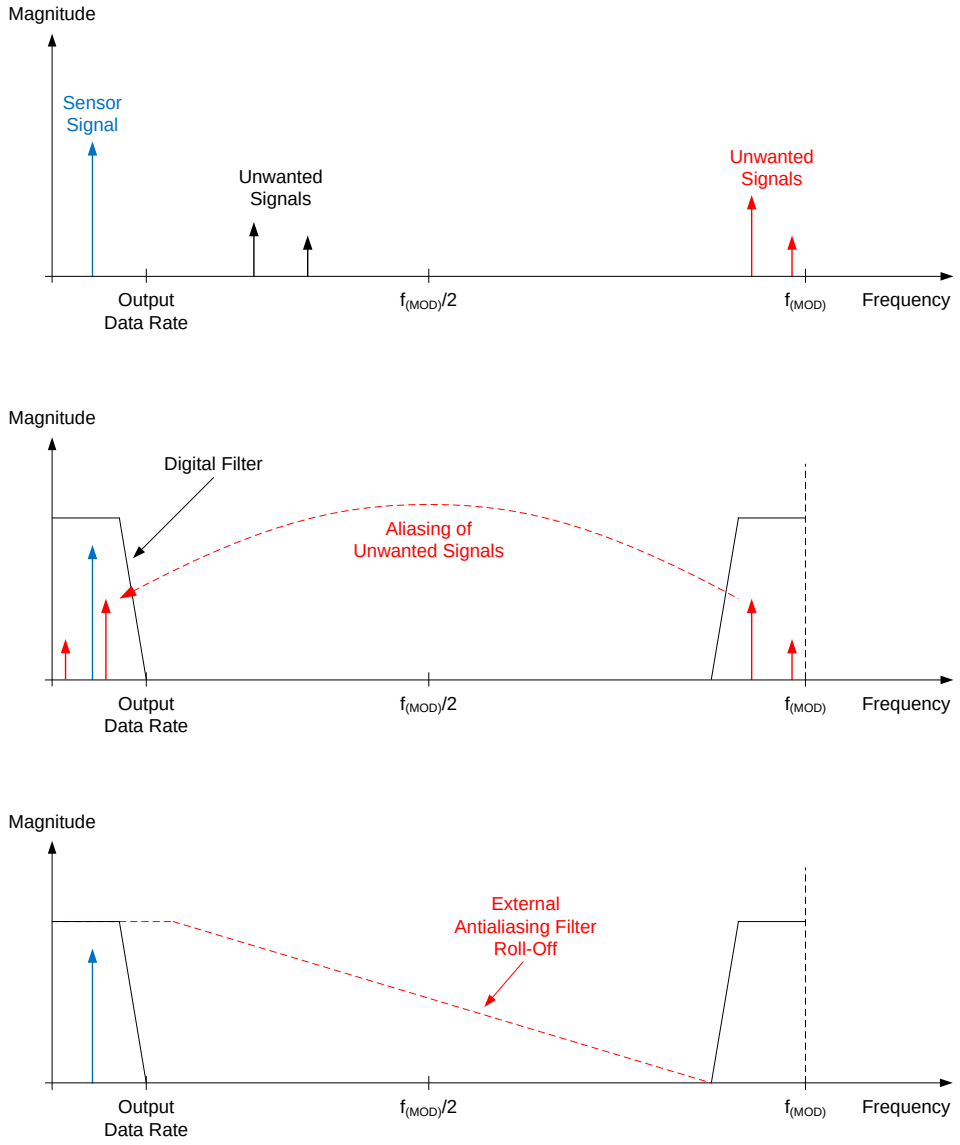


Figure 30. Effect of Aliasing

Application Information (continued)

Many sensor signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. In this case the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the MCA1220 attenuates signals to a certain degree, as illustrated in the filter response plots in the *Digital Filter* section. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10x higher is generally a good starting point for a system design.

Internal to the device, prior to the PGA inputs, is an EMI filter; . The cutoff frequency of this filter is approximately 31.8 MHz, which helps reject high-frequency interferences.

External Reference and Ratiometric Measurements

The full-scale range of the MCA1220 is defined by the reference voltage and the PGA gain (FSR = $\pm V_{ref}$ / Gain). An external reference can be used instead of the integrated 2.048-V reference to adapt the FSR to the specific system needs. An external reference must be used if V_{IN} > 2.048 V. For example, an external 5-V reference and an AVDD = 5 V are required in order to measure a single-ended signal that can swing between 0 V and 5 V.

The reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. Because current noise and drift are common to both the sensor measurement and the reference, these components cancel out in the ADC transfer function. The output code is only a ratio of the sensor element and the value of the reference resistor. The value of the excitation current source itself is not part of the ADC transfer function.

Establishing a Proper Common-Mode Input Voltage

The MCA1220 can be used to measure various types of input signal configurations: single-ended, pseudo-differential, and fully-differential signals (which can be either unipolar or bipolar). However, configuring the device properly for the respective signal type is important.

Signals where the negative analog input is fixed and referenced to analog ground ($V_{(AINN)}$ = 0 V) are commonly called *single-ended signals*. The common-mode voltage of a single-ended signal consequently varies between 0 V and V_{IN} / 2. If the PGA is disabled and bypassed, the common-mode input voltage of the ADS1220 can be as low as 100 mV below AVSS and as large as 100 mV above AVDD. Therefore, the PGA_BYPASS bit must be set in order to measure single-ended signals when a unipolar analog supply is used (AVSS = 0 V). Gains of 1, 2, and 4 are still possible in this configuration. Measuring a 0-mA to 20-mA or 4-mA to 20-mA signal across a load resistor of 100 Ω referenced to GND is a typical example. The ADS1220 can directly measure the signal across the load resistor using a unipolar supply, the internal 2.048-V reference, and gain = 1 when the PGA is bypassed.

If gains larger than 4 are needed to measure a single-ended signal, the PGA must be enabled. In this case, a bipolar supply is required for the ADS1220 to meet the common-mode voltage requirement of the PGA.

Signals where the negative analog input (AIN_N) is fixed at a voltage other the 0 V are referred to as *pseudo-differential signals*. The common-mode voltage of a pseudo-differential signal varies between $V_{(AINN)}$ and $V_{(AINN)}$ + V_{IN} / 2.

Fully-differential signals in contrast are defined as signals having a constant common-mode voltage where the positive and negative analog inputs swing 180° out-of-phase but have the same amplitude.

Application Information (continued)

The MCA1220 can measure pseudo-differential and fully-differential signals both with the PGA enabled or bypassed. However, the PGA must be enabled in order to use gains greater than 4. The common-mode voltage of the input signal must meet the input-common mode voltage restrictions of the PGA (as explained in the *PGA Common-Mode Voltage Requirements* section) when the PGA is enabled. Setting the common-mode voltage at or near (AVSS + AVDD) / 2 in most cases satisfies the PGA common-mode voltage requirements.

Signals where both the positive and negative inputs are always ≥ 0 V are called *unipolar signals*. These signals can in general be measured with the MCA1220 using a unipolar analog supply (AVSS = 0 V). As mentioned previously, the PGA must be bypassed in order to measure single-ended, unipolar signals when using a unipolar supply.

A signal is called *bipolar* when either the positive or negative input can swing below 0 V. A bipolar analog supply (such as AVDD = 2.5 V, AVSS = –2.5 V) is required in order to measure bipolar signals with the MCA1220. A typical application task is measuring a single-ended, bipolar ±10 V signal where AIN_N is fixed at 0 V while AIN_P swings between –10 V and 10 V. The ADS1220 cannot directly measure this signal because the 10 V exceeds the analog power-supply limits. However, one possible solution is to use a bipolar analog supply (AVDD = 2.5 V, AVSS = –2.5 V), gain = 1, and a resistor divider in front of the MCA1220. The resistor divider must divide the voltage down to ≤ ±2.048 V to be able to measure it using the internal 2.048-V reference.

Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog and reference inputs floating, or connect the inputs to mid-supply or to AVDD. AIN3/REFN1 is an exception. Leave the AIN3/REFN1 pin floating when not used in order to avoid accidently shorting the pin to AVSS through the internal low-side switch. Connecting unused analog or reference inputs to AVSS is possible as well, but can yield higher leakage currents than the previously mentioned options.

Do not float unused digital inputs; excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND, even when in power-down mode. If $\overline{CS}$ is not used, tie this pin to DGND. If the internal oscillator is used, tie the CLK pin to DGND. If the $\overline{DRDY}$ output is not used, leave the pin unconnected or tie the pin to DVDD using a weak pullup resistor.

Application Information (continued)

Pseudo Code Example

The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC in order to take subsequent readings from the ADS1220 in continuous conversion mode. The dedicated $\overline{DRDY}$ pin is used to indicate availability of new conversion data. The default configuration register settings are changed to gain = 16, continuous conversion mode, and simultaneous 50-Hz and 60-Hz rejection.

```
Power-up;
Delay to allow power supplies to settle and power-up reset to complete (minimum of 50 µs);
Configure the SPI interface of the microcontroller to SPI mode 1 (CPOL = 0, CPHA = 1);
If the CS pin is not tied low permanently, configure the microcontroller GPIO connected to CS as an
output;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt
input;
Set CS to the device low;
Delay for a minimum of t(CSSC);
Send the RESET command (06h) to make sure the device is properly reset after power-up;
Delay for a minimum of 50 µs + 32 · t(CLK);
Write the respective register configuration with the WREG command (43h, 08h, 04h, 10h, and 00h);
As an optional sanity check, read back all configuration registers with the RREG command (23h);
Send the START/SYNC command (08h) to start converting in continuous conversion mode;
Delay for a minimum of t(SCCS);
Clear CS to high (resets the serial interface);
Loop
{
    Wait for DRDY to transition low;
    Take CS low;
    Delay for a minimum of t(CSSC);
    Send 24 SCLK rising edges to read out conversion data on DOUT/DRDY;
    Delay for a minimum of t(SCCS);
    Clear CS to high;
}
Take CS low;
Delay for a minimum of t(CSSC);
Send the POWERDOWN command (02h) to stop conversions and put the device in power-down mode;
Delay for a minimum of t(SCCS);
Clear CS to high;
```

We recommends running an offset calibration before performing any measurements or when changing the gain of the PGA. The internal offset of the device can, for example, be measured by shorting the inputs to mid-supply (MUX[3:1] = 1110). The microcontroller then takes multiple readings from the device with the inputs shorted and stores the average value in the microcontroller memory. When measuring the sensor signal, the microcontroller then subtracts the stored offset value from each device reading to obtain an offset compensated result. Note that the offset can be either positive or negative in value.

Power Supply Recommendations

The device requires two power supplies: analog (AVDD, AVSS) and digital (DVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supply. The digital supply sets the digital I/O levels.

Power-Supply Sequencing

The power supplies can be sequenced in any order, but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage and current limits. Ramping DVDD together with or before AVDD minimizes any leakage current through AIN3/REFN1 because of the low-side switch connected to this input. If AVDD ramps before DVDD, then the low-side switch is in an unknown state and can short the AIN3/REFN1 input to AVSS until DVDD has ramped. Wait approximately 50 µs after all power supplies are stabilized before communicating with the device to allow the power-up reset process to complete.

Power-Supply Ramp Rate

For proper device power-up over the entire temperature range, the power-supply ramp rate must be monotonic and slower than 1 V per 50 µs, as shown in Figure 31.

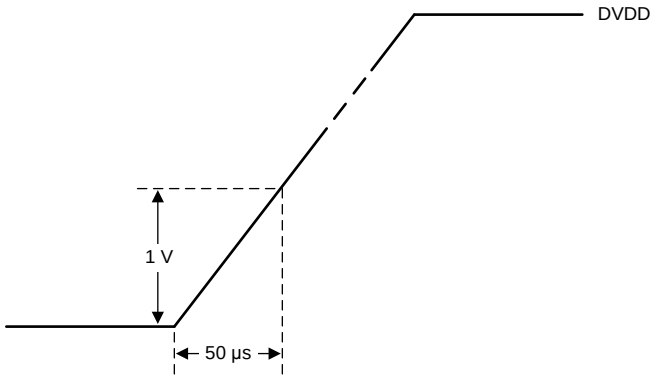


Figure 31. Power-Supply Ramp Rate

Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD, AVSS (when using a bipolar supply) and DVDD must be decoupled with at least a 0.1-µF capacitor, as shown in Figure 3 2 and Figure 33. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. We recommends connecting analog and digital ground together as close to the device as possible.

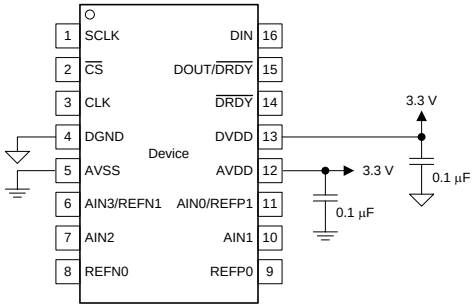


Figure 3 2 . Unipolar Analog Power Supply

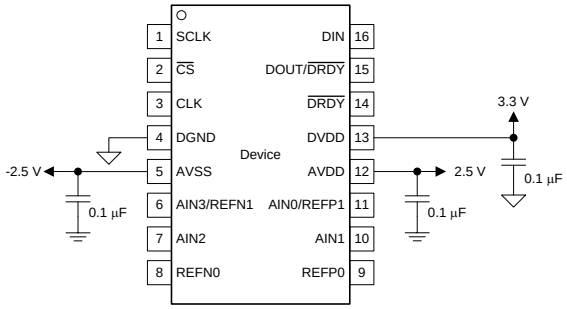


Figure 3 3 . Bipolar Analog Power Supply

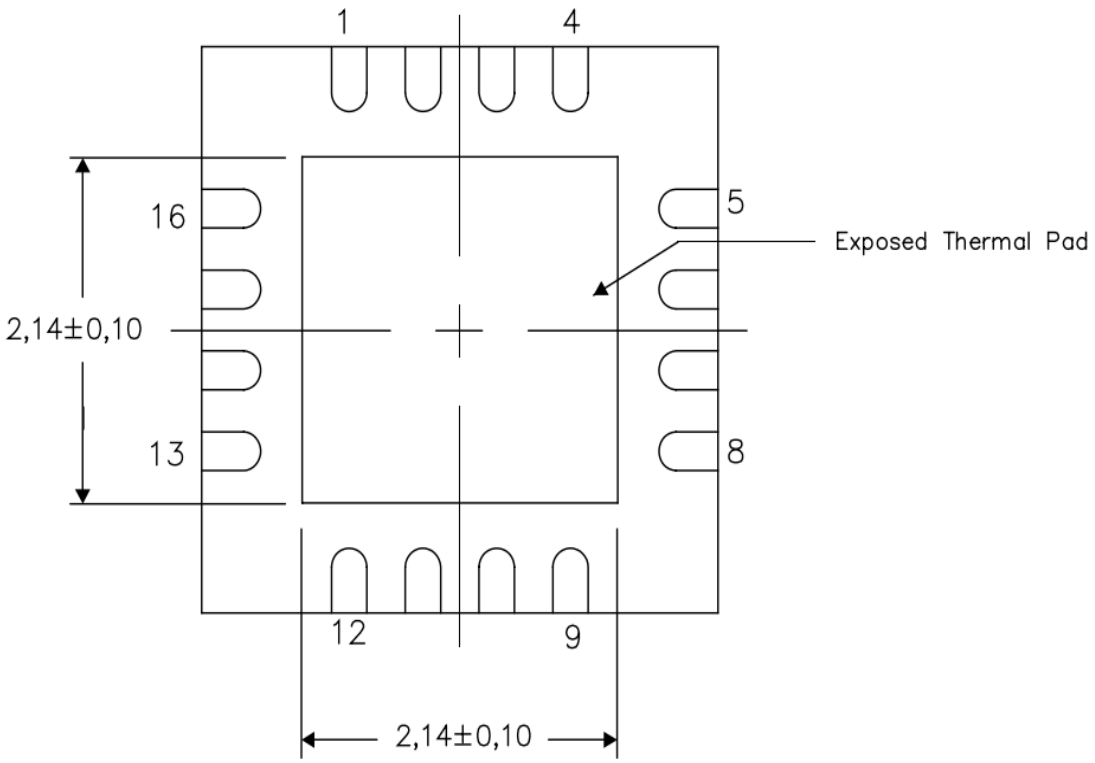


Figure 3 4 . VQFN-16 Package
All dimensions are in millimeters

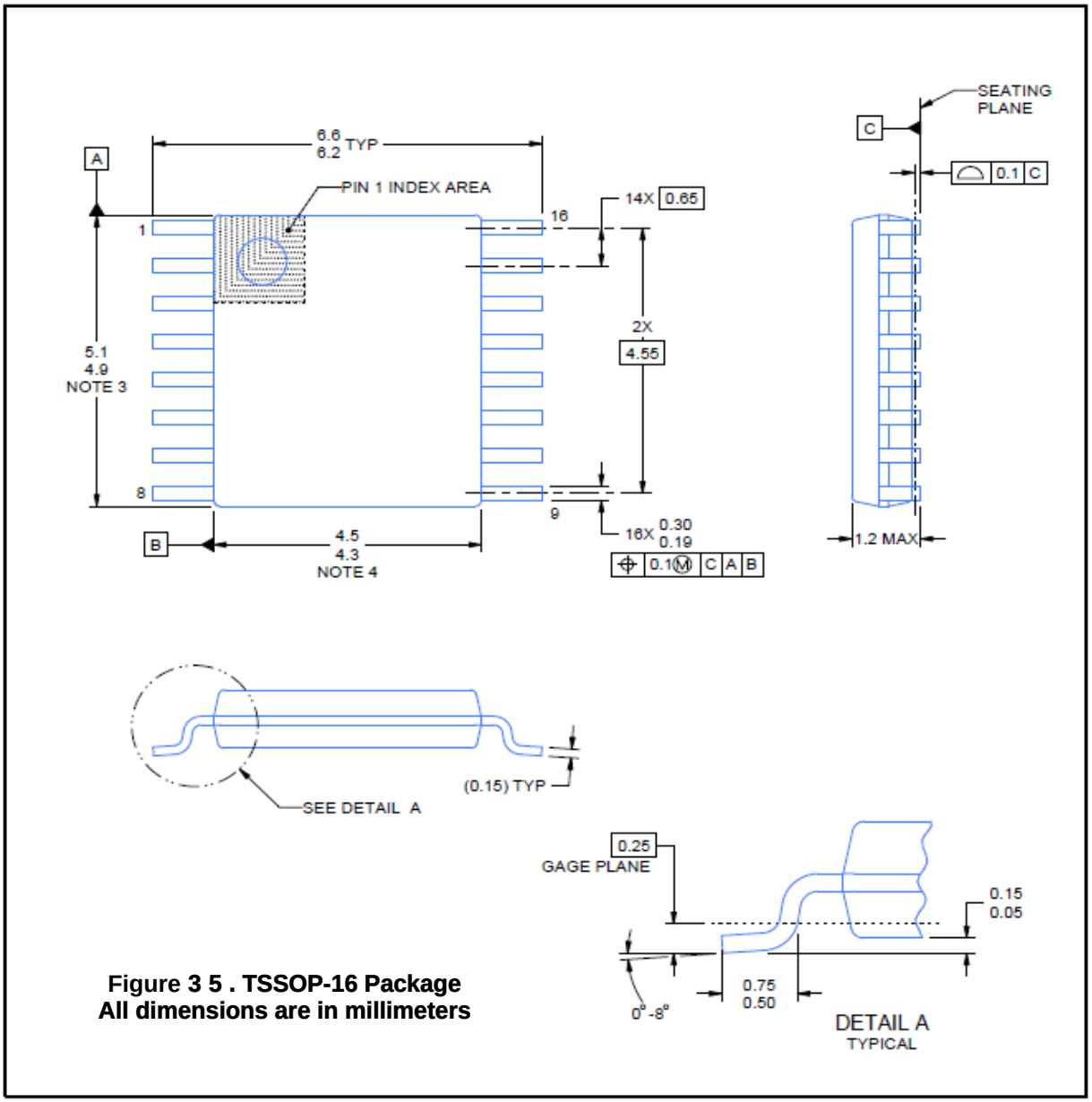


Figure 3 5 . TSSOP-16 Package
All dimensions are in millimeters

ORDERING INFORMATION

Mode[1]	Temperature Range	Package Description	Package Option
MCA1220VFN	–40°C ~+125°C	VQFN-16	Reel, 1000
MCA1220TSP	–40°C ~+125°C	TSSOP-16	Reel, 1000

[1]Z=RoHS Compliant Part.