Quad/Octal, Simultaneous Sampling, 24-Bit Analog-to-Digital Converters

FEATURES

- **Simultaneously Measure Four/Eight Channels**
- **Up to 144kSPS Data Rate**
- **AC Performance:**
  70kHz Bandwidth
  110dB SNR (High-Resolution Mode)
  –109dB THD
- **DC Accuracy:**
  0.8μV/°C Offset Drift
  1.3ppm/°C Gain Drift
- **Selectable Operating Modes:**
  High-Speed: 128kSPS, 106dB SNR
  High-Resolution: 52kSPS, 110dB SNR
  Low-Power: 52kSPS, 39mW/ch
  Low-Speed: 10kSPS, 9mW/ch
- **Linear Phase Digital Filter**
- **SPI™ or Frame-Sync Serial Interface**
- **Low Sampling Aperture Error**
- **Modulator Output Option (digital filter bypass)**
- **Analog Supply: 5V**
- **Digital Core: 1.8V**
- **I/O Supply: 1.8V to 3.3V**

APPLICATIONS

- **Vibration/Modal Analysis**
- **Multi-Channel Data Acquisition**
- **Acoustics/Dynamic Strain Gauges**
- **Pressure Sensors**

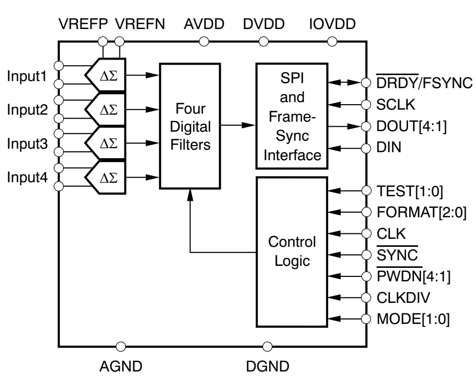
DESCRIPTION

Based on the single-channel architecture, the MCA1274 (quad) and MCA1278 (octal) are 24-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with data rates up to 144k samples per second (SPS), allowing simultaneous sampling of four or eight channels. The devices are offered in identical packages, permitting drop-in expandability.

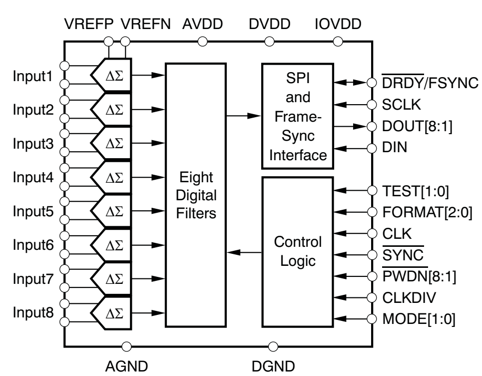
High-resolution ADCs in audio applications offer larger usable bandwidths, but the offset and drift specifications are significantly lower than respective industrial counterparts. The MCA1274 and MCA1278 combine these types of converters, allowing high-precision industrial measurement with excellent DC and AC specifications.

The high-order, chopper-stabilized modulator achieves very low drift with low in-band noise. The onboard decimation filter suppresses modulator and signal out-of-band noise. These ADCs provide a usable signal bandwidth up to 90% of the Nyquist rate with less than 0.005dB of ripple.

Four operating modes allow for optimization of speed, resolution, and power. All operations are controlled directly by pins; there are no registers to program. The devices are fully specified over the extended temperature range (–55°C to +210°C for MCA1278CQ64-H and MCA1274CQ64-H) and are available in plastic eTQFP-64 and ceramic CQFP-64 packages.



MCA1274



MCA1278

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted(1)

		MCA1274, MCA1278	UNIT
AVDD to AGND		–0.3 to +6.0	V
DVDD, IOVDD to DGND		–0.3 to +3.6	V
AGND to DGND		–0.3 to +0.3	V
Input current	Momentary	100	mA
	Continuous	10	mA
Analog input to AGND		–0.3 to AVDD + 0.3	V
Digital input or output to DGND		–0.3 to IOVDD + 0.3	V
Maximum junction temperature		+150	°C
Operating temperature range	MCA1274	–55 to +210	°C
	MCA1278	–55 to +210	°C
Storage temperature range		–60 to +210	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All specifications at AVDD = +5V, DVDD = +1.8V, IOVDD = +3.3V, f_{CLK} = 27MHz, VREFP = 2.5V, VREFN = 0V, and all channels active, unless otherwise noted.

PARAMETER		TESTCONDITIONS	T_A=-55℃ to 175℃ (HPQ)			T_A=210℃ (HCQ)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUTS									
Full-scale input voltage (FSR[1])		V_{IN} = (AINP – AINN)		±V_{REF}			±V_{REF}		V
Absolute input voltage		AINP or AINN to AGND	AGND – 0.1		AVDD + 0.1	AGND – 0.1		AVDD + 0.1	V
Common-mode input voltage (V_{CM})		V_{CM} = (AINP + AINN)/2		2.5			2.5		V
Differential input impedance	High-Speed mode[2]			14		14			kΩ
	High-Resolution mode			14		14			kΩ
	Low-Power mode			28		28			kΩ
	Low-Speed mode			140		140			kΩ
DC PERFORMANCE									
		Nomissing codes	24						Bits
Noise		fCLK = 32.768MHz		128,000			128,000		SPS[3]
		f_{CLK} = 27MHz		105,469			105,469		SPS
	High-Resolution mode			52,734			52,734		SPS
	Low-Power mode			52,734			52,734		SPS
	Low-Speed mode			10,547			10,547		SPS
Integral nonlinearity(INL)[4]		Differential input, V_{CM}=2.5V		±0.0003	±0.0015			±0.0014	% FSR[1]
Offset error				0.25	3			2	mV
Offset drift				0.8					μV/°C
Gain error				0.1	0.5			0.5	% FSR
Gain drift				1.3					ppm/°C
Noise	High-Speed mode	Shorted input		8.5	68			16	μV, rms
	High-Resolution mode	Shorted input		5.5	13			12	μV, rms
	Low-Power mode	Shorted input		8.5	21			16	μV, rms
	Low-Speed mode	Shorted input		8.0	21			16	μV, rms
Common-mode rejection		f_{CM} = 60Hz	90	108		90			dB
Power-supply rejection	AVDD	f_{PS} = 60Hz		80			80		dB
	DVDD			85			85		dB
	IOVDD			105			105		dB
V_{COM} output voltage		No load		AVDD/2				AVDD/2	V

(1) FSR = full-scale range = $2V_{REF}$.
(2) f_{CLK} = 32.768MHz max for High-Speed mode, and 27MHz max for all other modes.
(3) SPS = samples per second.
(4) Best fit method.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at AVDD = +5V, DVDD = +1.8V, IOVDD = +3.3V, f_{CLK} = 27MHz, VREFP = 2.5V,VREFN = 0V, and all channels active, unless otherwise noted.

PARAMETER		TESTCONDITIONS	TA=-55℃ to 175℃			TA=210℃			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
		交流特性							
		f=1kHz, -0.5dBFS(5)		–107					dB
Signal-to-noise ratio (SNR)(6)	High-Speed mode		88	106		101			dB
	High-Resolution mode	V_{REF} = 2.5V	101	110		103			dB
		V_{REF} = 3V		111					dB
	Low-Power mode		98	106		100			dB
	Low-Speed mode		98	107		101			dB
Total harmonic distortion (THD)(7)		V_{IN} = 1kHz, –0.5dBFS		–108	–96			–96	dB
Spurious-free dynamic range				109					dB
Passband ripple				±0.005					dB
Passband				0.453f_{DATA}					Hz
–3dB Bandwidth				0.49f_{DATA}					Hz
Stop band attenuation	High-Resolution mode		95						dB
	All other modes		100						
Stop band	High-Resolution mode		0.547 f_{DATA}		127.453f_{DATA}				Hz
	All other modes		0.547 f_{DATA}		63.453 f_{DATA}				Hz
Group delay	High-Resolution mode			39/ f_{DATA}					s
	All other modes			38/ f_{DATA}					s
Settling time (latency)	High-Resolution mode	Complete settling		78/ f_{DATA}					s
	All other modes	Complete settling		76/ f_{DATA}					s
		VOLTAGE REFERENCE INPUTS							
Negative reference input(VREFN)			AGND – 0.1		AGND + 0.1	AGND – 0.1		AGND + 0.1	V
Reference input voltage (V_{REF})(8) (V_{REF} = VREFP – VREFN)		0.1 ≤ f_{CLK} ≤ 27MHz	0.5	2.5	3.1	0.5	2.5	3.1	V
		27 < f_{CLK} ≤ 32.768MHz	0.5	2.5	2.6	0.5	2.5	2.6	V
MCA1274 Reference Input impedance	High-Speed mode			1.3			1.3		kΩ
	High-Resolution mode			1.3			1.3		kΩ
	Low-Power mode			2.6			2.6		kΩ
	Low-Speed mode			13			13		kΩ
MCA1278 Reference Input impedance	High-Speed mode			0.65			0.		kΩ
	High-Resolution mode			0.65			650.		kΩ
	Low-Power mode			1.3			65		kΩ
	Low-Speed mode			6.5			1.3		kΩ
		DIGITAL INPUT/OUTPUT (IOVDD=1.8V to 3.6V)					6.5		
V_{IH}			0.7 IOVDD		IOVDD	0.7 IOVDD		IOVDD	V
V_{IL}			DGND		0.3 IOVDD	DGND		0.3 IOVDD	V
V_{OH}		I_{OH} = 4mA	0.8 IOVDD		IOVDD	0.8 IOVDD		IOVDD	V
V_{OL}		I_{OL} = 4mA	DGND		0.2 IOVDD	DGND		0.2 IOVDD	V
Input leakage		0 < $V_{IN\ DIGITAL}$ < IOVDD			±10				μA
Master clock rate (f_{CLK})		High-Speed mode(8)	0.1		32.768	0.1		32.768	MHz
		Other modes	0.1		27	0.1		27	MHz

(5) Worst-case channel crosstalk between one or more channels.
(6) Minimum SNR is ensured by the limit of the *DC noise* specification.
(7) THD includes the first nine harmonics of the input signal; Low-Speed mode includes the first five harmonics.
(8) f_{CLK} = 32.786MHz max for High-Speed mode, and 27MHz max for all other modes.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at AVDD = +5V, DVDD = +1.8V, IOVDD = +3.3V, f_{CLK} = 27MHz, VREFP = 2.5V,VREFN = 0V, and all channels active, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A=-55℃ to 175℃			T_A=210℃			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY									
AVDD			4.75	5	5.25	4.75	5	5.25	V
DVDD(9)			1.65	1.8	1.95	1.65	1.8	1.95	V
IOVDD			1.65		3.6	1.65		3.6	V
Power-down current	AVDD			40	60		65		μA
	DVDD			50	85		200		μA
	IOVDD			24	40		25		μA
MCA1274									
MCA1274 AVDD current	High-Speed mode			65	65				mA
	High-Resolution mode			65	75				mA
	Low-Power mode			29	34				mA
	Low-Speed mode			6.5	8.5				mA
MCA1274 DVDD current	High-Speed mode			11.5	15				mA
	High-Resolution mode			8	10				mA
	Low-Power mode			6	8.5				mA
	Low-Speed mode			1.75	2.25				mA
MCA1274 IOVDD current	High-Speed mode			0.25	0.55				mA
	High-Resolution mode			0.15	0.3				mA
	Low-Power mode			0.15	0.3				mA
	Low-Speed mode			0.05	0.25				mA
MCA1274 Power dissipation	High-Speed mode			265	402.				mW
	High-Resolution mode			257.	5392.				mW
	Low-Power mode			5122.	5				mW
	Low-Speed mode			5	220				mW
MCA1278				25	44.5				
MCA1278 AVDD current				130	150		168.	231.25	mA
				130	150		75168.	231.25	mA
				58	68		75	105	mA
				13	17		75	27.5	mA
MCA1278 DVDD current				23	30		15	31	mA
				16	20		24	20	mA
				12	17		17	17	mA
				3.5	4.5		13	5	mA
MCA1278 IOVDD current				0.5	1.1		3	1.15	mA
				0.3	0.6		0.3	0.75	mA
				0.3	0.6		0.2	0.75	mA
				0.1	0.5		0.2	0.45	mA
MCA1278 Power dissipation				530	805		0.1	1182	mW
				515	785			1182	mW
				245	440			546	mW
				50	89			144	mW

(9) f_{CLK} = 32.768MHz max for High-Speed mode, and 27MHz max for all other modes.

MCA1274/MCA1278 PIN ASSIGNMENTS

HCQ64
(TOP VIEW)

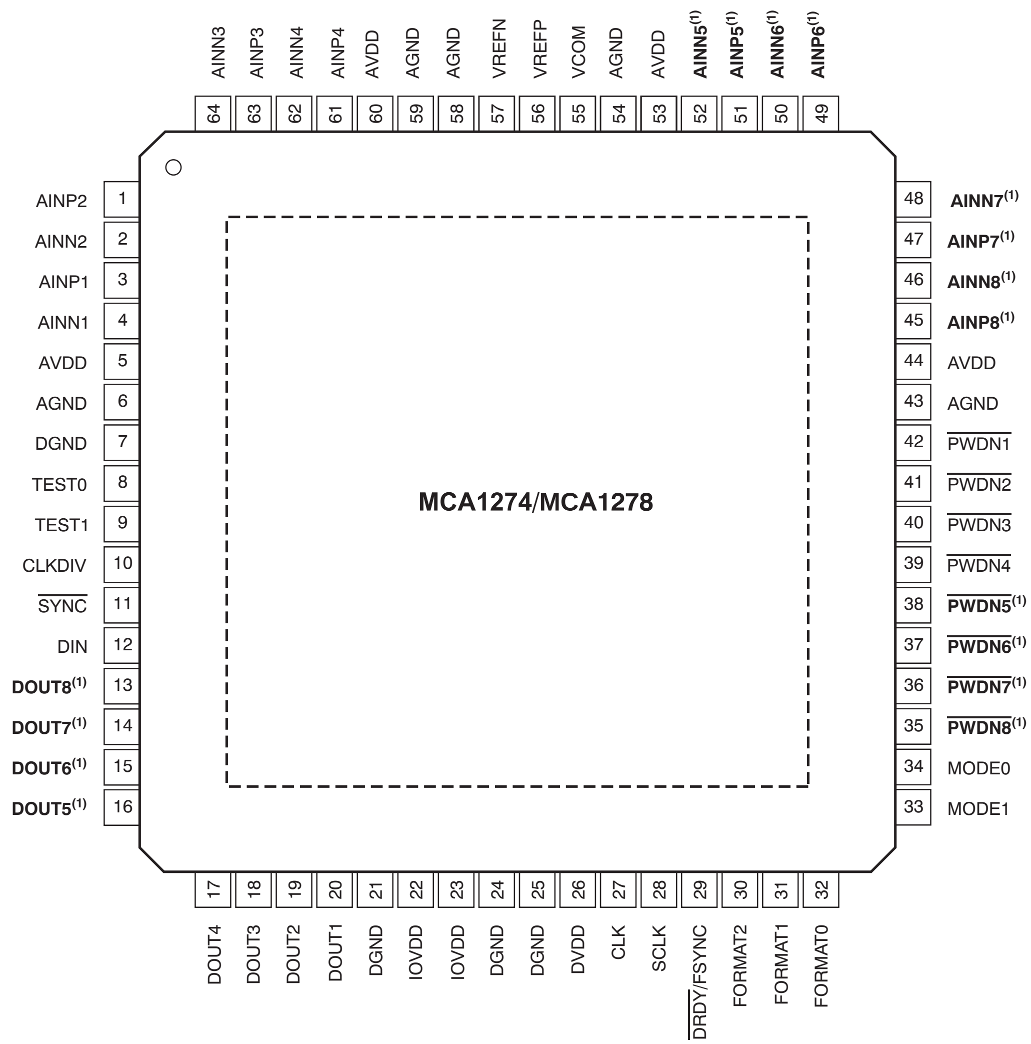


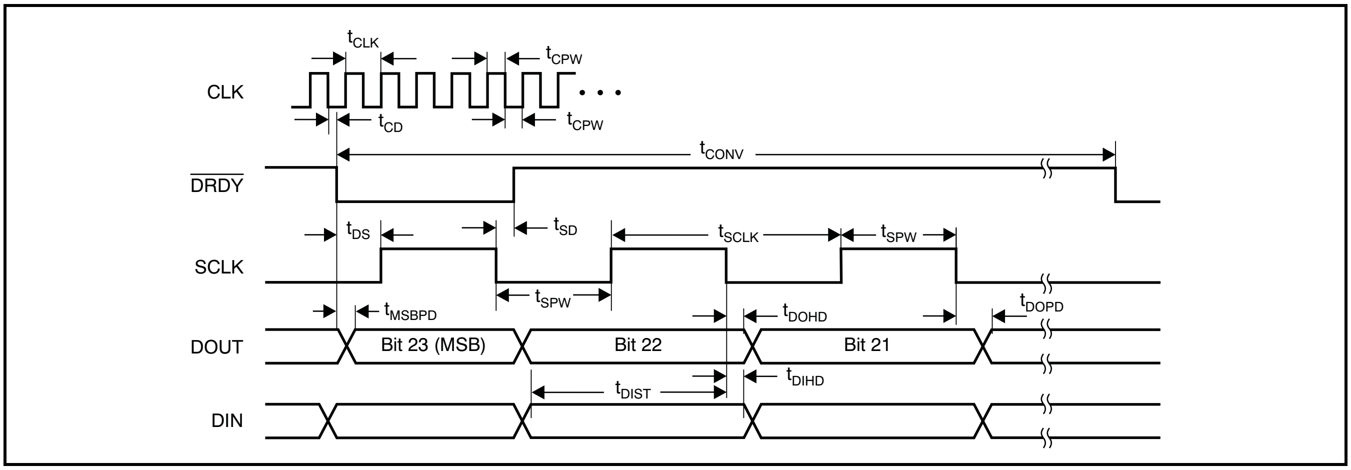
Table 1. MCA1274/MCA1278 PIN DESCRIPTIONS

PIN			
NAME	**NO.**	**FUNCTION**	**DESCRIPTION**
AGND	6, 43, 54, 58, 59	Analog ground	Analog ground; connect to DGND using a single plane.
AINP1	3	Analog input	**MCA1278:** AINP[8:1] Positive analog input, channels 8 through 1. **MCA1274:** AINP[8:5] Connected to internal ESD rails. The inputs may float. AINP[4:1] Positive analog input, channels 4 through 1.
AINP2	1	Analog input	
AINP3	63	Analog input	
AINP4	61	Analog input	
AINP5	51	Analog input	
AINP6	49	Analog input	
AINP7	47	Analog input	
AINP8	45	Analog input	

Table 1. MCA1274/MCA1278 PIN DESCRIPTIONS (continued)

PIN			
NAME	NO.	FUNCTION	DESCRIPTION
AINN1	4	Analog input	**MCA1278:** AINN[8:1] Negative analog input, channels 8 through 1. **MCA1274:** AINN[8:5] Connected to internal ESD rails. The inputs may float. AINN[4:1] Negative analog input, channels 4 through 1.
AINN2	2	Analog input	
AINN3	64	Analog input	
AINN4	62	Analog input	
AINN5	52	Analog input	
AINN6	50	Analog input	
AINN7	48	Analog input	
AINN8	46	Analog input	
AVDD	5, 44, 53, 60	Analog power supply	Analog power supply (4.75V to 5.25V).
VCOM	55	Analog output	AVDD/2 Unbuffered voltage output.
VREFN	57	Analog input	Negative reference input.
VREFP	56	Analog input	Positive reference input.
CLK	27	Digital input	Master clock input (f_{CLK}).
CLKDIV	10	Digital input	CLK input divider control: 1 = 32.768MHz (High-Speed mode)/otherwise 27MHz 0 = 13.5MHz (low-power)/5.4MHz (low-speed)
DGND	7, 21, 24, 25	Digital ground	Digital ground power supply.
DIN	12	Digital input	Daisy-chain data input.
DOUT1	20	Digital output	DOUT1 is TDM data output (TDM mode). **MCA1278:** DOUT[8:1] Data output for channels 8 through 1. **MCA1274:** DOUT[8:5] Internally connected to active circuitry; outputs are driven. DOUT[4:1] Data output for channels 4 through 1.
DOUT2	19	Digital output	
DOUT3	18	Digital output	
DOUT4	17	Digital output	
DOUT5	16	Digital output	
DOUT6	15	Digital output	
DOUT7	14	Digital output	
DOUT8	13	Digital output	
$\overline{\text{DRDY}}$/ FSYNC	29	Digital input/output	Frame-Sync protocol: frame clock input; SPI protocol: data ready output.
DVDD	26	Digital power supply	Digital core power supply.
FORMAT0	32	Digital input	FORMAT[2:0] Selects Frame-Sync/SPI protocol, TDM/discrete data outputs, fixed/dynamic position TDM data, and modulator mode/normal operating mode.
FORMAT1	31	Digital input	
FORMAT2	30	Digital input	
IOVDD	22, 23	Digital power supply	I/O power supply (+1.65V to +3.6V).
MODE0	34	Digital input	MODE[1:0] Selects High-Speed, High-Resolution, Low-Power, or Low-Speed mode operation.
MODE1	33	Digital input	
$\overline{\text{PWDN1}}$	42	Digital input	**MCA1278:** $\overline{\text{PWDN}}$[8:1] Power-down control for channels 8 through 1. **MCA1274:** $\overline{\text{PWDN}}$[8:5] must = 0V. PWDN[4:1] Power-down control for channels 4 through 1.
$\overline{\text{PWDN2}}$	41	Digital input	
$\overline{\text{PWDN3}}$	40	Digital input	
$\overline{\text{PWDN4}}$	39	Digital input	
$\overline{\text{PWDN5}}$	38	Digital input	
$\overline{\text{PWDN6}}$	37	Digital input	
$\overline{\text{PWDN7}}$	36	Digital input	
$\overline{\text{PWDN8}}$	35	Digital input	
SCLK	28	Digital input/output	Serial clock input, Modulator clock output.
$\overline{\text{SYNC}}$	11	Digital input	Synchronize input (all channels).
TEST0	8	Digital input	TEST[1:0] Test mode select: 00 = Normal operation, 11 = Test mode, 01 = Do not use, 10 = Do not use
TEST1	9	Digital input	

SPI FORMAT TIMING



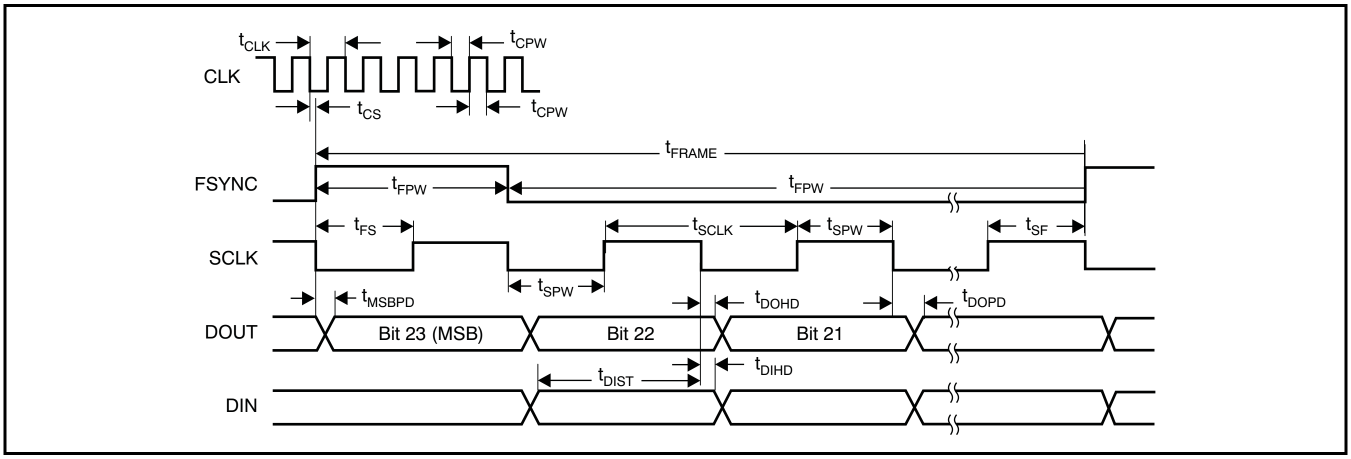
SPI FORMAT TIMING SPECIFICATION

For T_A = –40°C to +105°C, IOVDD = 1.65V to 3.6V, and DVDD = 1.65V to 1.95V, unless otherwise noted.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)(1)	37		10,000	ns
t_{CPW}	CLK positive or negative pulse width	15			ns
t_{CONV}	Conversion period ($1/f_{DATA}$)(2)	256		2560	t_{CLK}
t_{CD}(3)	Falling edge of CLK to falling edge of $\overline{DRDY}$		22		ns
t_{DS}(3)	Falling edge of $\overline{DRDY}$ to rising edge of first SCLK to retrieve data	1			t_{CLK}
t_{MSBPD}	$\overline{DRDY}$ falling edge to DOUT MSB valid (propagation delay)			16	ns
t_{SD}(3)	Falling edge of SCLK to rising edge of $\overline{DRDY}$		18		ns
t_{SCLK}(4)	SCLK period	1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width	0.4			t_{CLK}
t_{DOHD}(3)(5)	SCLK falling edge to new DOUT invalid (hold time)	10			ns
t_{DOPD}(3)	SCLK falling edge to new DOUT valid (propagation delay)			32	ns
				26	ns(6)
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)	6			ns
t_{DIHD}(5)	Old DIN valid to falling edge of SCLK (hold time)	6			ns

(1) f_{CLK} = 27MHz maximum.
(2) Depends on MODE[1:0] and CLKDIV selection.
(3) Load on $\overline{DRDY}$ and DOUT = 20pF.
(4) For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc.
(5) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is > 4ns.
(6) DOUT1, TDM mode, IOVDD = 3.15V to 3.45V, and DVDD = 1.7V to 1.9V.

FRAME-SYNC FORMAT TIMING



FRAME-SYNC FORMAT TIMING SPECIFICATION

For T_A = –40°C to +105°C, IOVDD = 1.65V to 3.6V, and DVDD = 1.65V to 2.2V, unless otherwise noted.

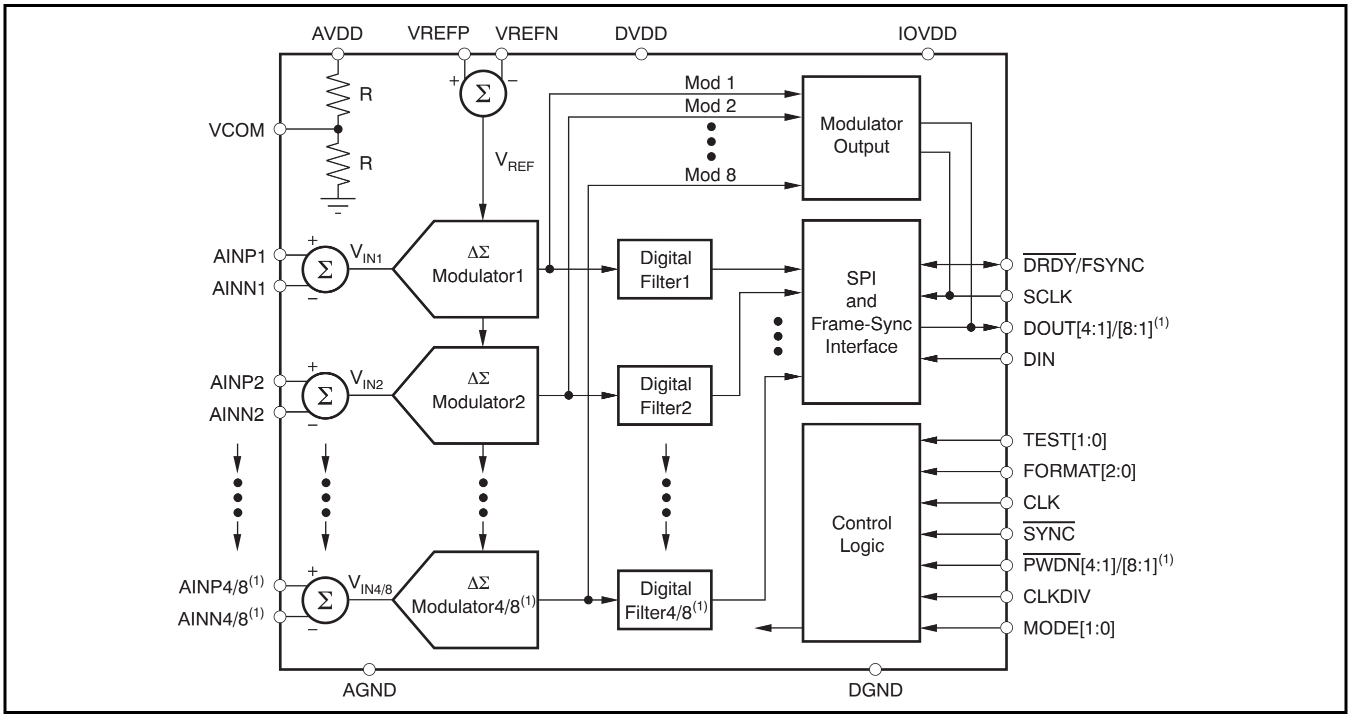
SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)	High-Speed mode	27		10,000	ns
		Other modes	37		10,000	ns
t_{CPW}	CLK positive or negative pulse width		11			ns
t_{CS}	Falling edge of CLK to falling edge of SCLK		–0.25		0.25	t_{CLK}
t_{FRAME}	Frame period ($1/f_{DATA}$)(1)		256		2560	t_{CLK}
t_{FPW}	FSYNC positive or negative pulse width		1			t_{SCLK}
t_{FS}	Rising edge of FSYNC to rising edge of SCLK		5			ns
t_{SF}	Rising edge of SCLK to rising edge of FSYNC		5			ns
t_{SCLK}	SCLK period(2)		1			t_{CLK}
t_{SPW}	SCLK positive or negative pulse width		0.4			t_{CLK}
t_{DOHD}(3)(4)	SCLK falling edge to old DOUT invalid (hold time)		10			ns
t_{DOPD}(4)	SCLK falling edge to new DOUT valid (propagation delay)				31	ns
					21	ns(5)
					25	ns(6)
t_{MSBPD}	FSYNC rising edge to DOUT MSB valid (propagation delay)				31	ns
					21	ns(5)
					25	ns(6)
t_{DIST}	New DIN valid to falling edge of SCLK (setup time)		6			ns
t_{DIHD}(3)	Old DIN valid to falling edge of SCLK (hold time)		6			ns

(1) Depends on MODE[1:0] and CLKDIV selection.
(2) SCLK must be continuously running and limited to ratios of 1, 1/2, 1/4, and 1/8 of f_{CLK}.
(3) t_{DOHD} (DOUT hold time) and t_{DIHD} (DIN hold time) are specified under opposite worst-case conditions (digital supply voltage and ambient temperature). Under equal conditions, with DOUT connected directly to DIN, the timing margin is > 4ns.
(4) Load on DOUT = 20pF.
(5) DOUT1, TDM mode, IOVDD = 3.15V to 3.45V, and DVDD = 2V to 2.2V.
(6) DOUT1, TDM mode, IOVDD = 3.15V to 3.45V, and DVDD = 1.7V to 1.9V.

OVERVIEW

The MCA1274 (quad) and MCA1278 (octal) are 24-bit, delta-sigma ADCs based on the Δ-Σ architecture. They offer the combination of outstanding DC accuracy and superior AC performance. The figure below shows the block diagram. Note that both devices are functionally the same, except that the MCA1274 has four ADCs and the MCA1278 has eight ADCs. The packages are identical, and the MCA1274 pinout is compatible with the MCA1278, permitting true drop-in expandability. The converters are comprised of four (MCA1274) or eight (MCA1278) 6th-order, delta-sigma modulators followed by low-ripple, linear-phase FIR filters. The modulators measure the differential input signal, VIN = (AINP – AINN), against the differential reference, VREF = (VREFP – VREFN). The digital filters receive the modulator signal and provide a low-noise digital output. To allow trade-offs among speed, resolution, and power, four operating modes are supported: high-speed, high-resolution, low-power, and low-speed. The table below summarizes the performance of each mode. In high-speed mode, the maximum data rate is 144kSPS. In high-resolution mode, the SNR = 111dB (VREF = 3.0V); in low-power mode, the power consumption is only 31mW per channel; in low-speed mode, the power consumption at 10.5kSPS is only 7mW per channel. Users can also bypass the digital filter and directly access the modulator output.

The MCA1274/MCA1278 are configured by simply setting the appropriate I/O pins; no register programming is required. A serial interface supports data retrieval in both SPI and frame-sync formats. The MCA1274/MCA1278 feature a daisy-chain output and external synchronization capability, facilitating easy use in systems requiring more than eight channels.



(1) The MCA1274 has four channels; the MCA1278 has eight channels.

MCA1274/MCA1278 Block Diagram

Table 2. Operating Mode Performance Summary

MODE	MAX DATA RATE (SPS)	PASSBAND (kHz)	SNR (dB)	NOISE (μV_{RMS})	POWER/CHANNEL (mW)
High-Speed	128,000	57,984	106	8.5	70
High-Resolution	52,734	23,889	110	5.5	64
Low-Power	52,734	23,889	106	8.5	31
Low-Speed	10,547	4,798	107	8.0	7

FUNCTIONAL DESCRIPTION

The MCA1274/MCA1278 is a - ADC composed of four /eight independent converters that sample the input signals in parallel. Each converter consists oftwo main functional blocks that perform the ADC conversion: a modulator and a digital filter.The modulator samples the input signalwhile simultaneously sampling the reference voltage to produce a digital output. The density ofthe digital code transitions is proportional to the analog input level relative to the reference voltage. The pulse stream is filtered by an internal digitalfilter, which generates the output conversion result.

During operation, the modulator samples the input signal at a high rate (typically 64 times higher than the final output data rate). The quantization noise of the modulator is shifted to higher frequency ranges and is subsequently removed by the internal digital filter. Over sampling results in very low noise levels within the signal passband. Since the input signal is sampled at a very high rate, input signal aliasing does not occur until the input signal frequency approaches the modulator sampling rate. Due to the high modulator sampling rate, this architecture significantly relaxes the requirements for external anti -aliasing filters.

SAMPLING APERTURE MATCHING

The MCA1274/MCA1278 converters operate from the same CLK input. The CLK input controls the timing of the modulator sampling instants. The converters are designed to control sampling skew between channels or modulator sampling aperture matching. Additionally , the digital filters are synchronized to begin the convolution phase on the same modulator clock cycle. This design enables good phase matching between the channels of the MCA1274/MCA1278.
Phase matching between a 4-channel MCA1274 and another MCA1274(for a total of eight or more channels) may not exhibit the same degree of sampling matching. Due to variations in manufacturing, the resulting differences in internal clock signal coupling and the variance of the external CLK signal to each chip can lead to larger sampling matching errors. Clock traces of equal length or external clock distribution chips can be used to reduce inter-chip sampling matching errors.

FREQUENCY RESPONSE

The digital filter establishes the overall frequency response. Employing a multi-stage FIR topology, the filter provides linear phase with minimal passband ripple and high stopband attenuation. The oversampling ratio of the digital filter (i.e., the ratio of modulator sampling rate to output data rate, or f_{MOD} / f_{DATA}) is selectable by mode.

Table 3. Oversampling Ratio versus Mode

MODE SELECTION	OVERSAMPLING RATIO (f_{MOD}/f_{DATA})
High-Speed	64
High-Resolution	128
Low-Power	64
Low-Speed	64

Table 4. High-Speed Mode f_{CLK} Conditions

f_{CLK} (MHz)	V_{REF} (V)	DVDD (V)	INTERFACE
$0.1 \le f_{CLK} \le 27$	0.5 to 3.1	1.65 to 1.95	Frame-Sync or SPI
$27 < f_{CLK} \le 32.768$	0.5 to 2.6	1.65 to 1.95	Frame-Sync

CLOCK INPUT (CLK)

Operation of the MCA1274/MCA1278 requires a clock input. Each converter of the MCA1274/ MCA1278 operates from the same clock input.For the maximum data rate, the clock input is 27 MHz or 13.5 MHz in low-power mode, and 27 MHz or 5.4 MHz in low-speed mode, depending on the setting of the CLKDIV input. For high-speed mode, the maximum CLK input frequency is 32.768 MHz. For high-resolution mode, the maximum CLK input frequency is 27 MHz. Operation in high-speed mode is limited by the clock input frequency.

The choice of external clock frequency (f_{CLK}) does not affect the resolution of the MCA1274/MCA1278. Using a lower f_{CLK} frequency can reduce the power consumption of the external clock buffer. The output data rate is proportional to the clock frequency, with a minimum at f_{CLK} = 100 kHz. The table below summarizes the ratio of clock frequency (f_{CLK}) to data rate (f_{DATA}), the maximum data rate, and the corresponding maximum clock input for the four operating modes.As with any high-speed data converter, a high-quality, low-jitter clock is essential to ensure optimum performance. Preventing clock input overdrive, keeping clock traces as short as possible, and using a 50Ω series resistor close to the source generally improve overall system performance.

Table 5 . Clock Input Options

MODE SELECTION	MAX f_{CLK} (MHz)	CLKDIV	f_{CLK}/f_{DATA}	DATA RATE (SPS)
High-Speed	32.768	1	256	128,000
High-Resolution	27	1	512	52,734
Low-Power	27	1	512	52,734
	13.5	0	256	
Low-Speed	27	1	2,560	10,547
	5.4	0	512	

MODE SELECTION (MODE)

The MCA1274/78 support four operating modes: High-Speed, High-Resolution, Low-Power, and Low-Speed modes. These modes provide optimization of speed, resolution, and power consumption. The modeis selected by the status of the digital input pins MODE[1 :0]. The MCA1274/78 continuously monitor the status of the MODE pins during operation .

Table 6. Mode Selection

MODE[1:0]	MODE SELECTION	MAX f_{DATA} (1)
00	High-Speed	128,000
01	High-Resolution	52,734
10	Low-Power	52,734
11	Low-Speed	10,547

(1) f_{CLK} = 27MHz max (32.768MHz max in High-Speed mode).

When using the SPI protocol, $\overline{\text{DRDY}}$ is held high after a mode change occurs until settled (or valid) data are ready;

In Frame-Sync protocol, the DOUT pins are held low after a mode change occurs until settled data are ready; see Figure 2 and Table 7. Data can be read from the device to detect when DOUT changes to logic 1, indicating that the data are valid.

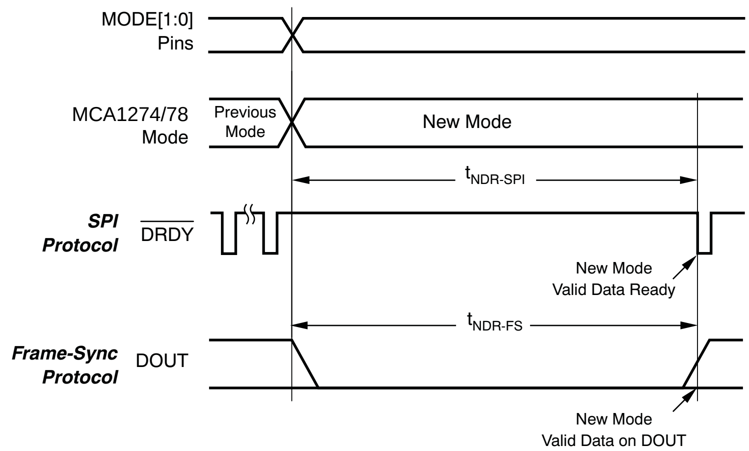


Figure 2. Mode Change Timing

Table 7. New Data After Mode Change

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{NDR-SPI}$	Time for new data to be ready (SPI)			129	Conversions ($1/f_{DATA}$)
t_{NDR-FS}	Time for new data to be ready (Frame-Sync)(1)	127		128	Conversions ($1/f_{DATA}$)

(1) If mode change is asynchronous to the FSYNC clock, t_{NDR-FS} varies from 127 to 128 conversions. If the mode change is made synchronous to FSYNC, t_{NDR-FS} is stable.

SYNCHRONIZATION (SYNC)

The MCA1274/78 can be synchronized by pulsing the SYNC pin low and then returning the pin high. When the pin goes low, the conversion process stops, and the internal counters used by the digital filter are reset. When the SYNC pin returns high, the conversion process restarts. Synchronization allows the conversion to be aligned with an external event, such as the changing of an external multiplexer on the analog inputs, or by a reference timing pulse.

Because the MCA1274/78 converters operate in parallel from the same master clock and use the same SYNC input control, they are always in synchronization with each other. The aperture match among internal channels is typically less than 500ps. However, the synchronization of multiple devicesis somewhat different. At device power-on, variations in internal reset thresholds from device to device may result in uncertainty inconversion timing.

The SYNC pin can be used to synchronize multiple devices to within the same CLK cycle. Figure 3 illustrates the timing requirement of SYNC and CLK in SPI format.

See Figure 4 for the Frame-Sync format timing requirement.

After synchronization, indication of valid data depends on whether SPI or Frame-Sync format was used.

In the SPI format, DRDY goes high as soon as SYNC is taken low; see Figure 3. After SYNC is returned high, DRDY stays high while the digital filter is settling. Once valid data are ready for retrieval, DRDY goes low.

In the Frame-Sync format, DOUT goes low as soon as SYNC is taken low; see Figure 4. After SYNC is returned high, DOUT stays low while the digital filter is settling. Once valid data are ready for retrieval, DOUT begins to output valid data. For proper synchronization, FSYNC, SCLK, and CLK must be established before taking SYNC high, and must then remain running. If the clock inputs (CLK, FSYNC or SCLK) are subsequently interrupted or reset, re-assert the SYNC pin.

For consistent performance, re-assert SYNC after device power-on when data first appear.

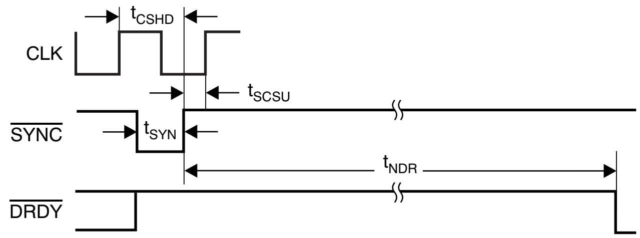


Figure 3. Synchronization Timing (SPI Protocol)

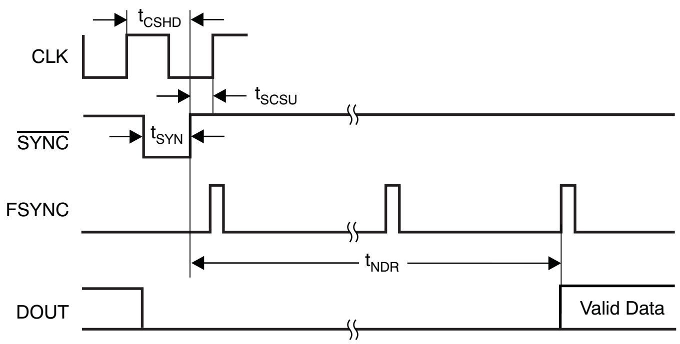


Figure 4. Synchronization Timing (Frame-Sync Protocol)

POWER-DOWN (PWDN)

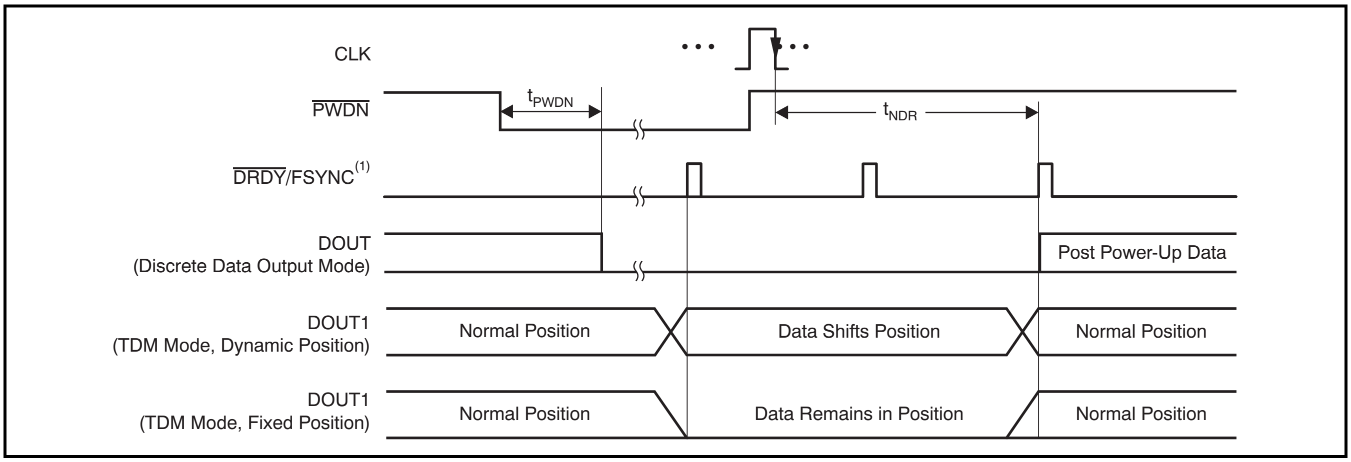
The channels of the MCA1274/78 can be independently powered down by use of the PWDN inputs. To enter the power-down mode, hold the respective PWDN pin low for at least two CLK cycles. To exit power-down, return the corresponding PWDN pin high. Note that when all channels are powered down, the MCA1274/78 enters a microwatt (μ W)power state where all internal biasing is disabled . In this state, the TEST[1:0] input pins must be driven ; all other input pins can float. The MCA1274/ 78 outputs remain driven.

As shown in Figure 5 and Table 8, a maximum of 130 conversion cycles must elapse for SPI interface, and 129 conversion cycles must elapse for Frame-Sync, before reading data after exiting power-down. Data from channels already running are not affected. The user software can perform the required delay time in any of the following ways:

1. Count the number of data conversions after taking the PWDN pin high.
2. Delay $129/f_{DATA}$ or $130/f_{DATA}$ after taking the PWDN pins high, then read data.
3. Detect for non-zero data in the powered-up channel.

After one or multiple channels are powered up, these channels are synchronized with each other. The use of the SYNC pin is not required to synchronize them. When a channel is powered down in TDM data format , the data from that channel is either forced to zero (in fixed-position TDM data mode) or replaced by shifting data from the next channel into the idle data position (in dynamic-position TDM data mode). In discrete data format, the data is always forced to zero.

When a channel is powered up in dynamic-position TDM data format mode, the channel data remains packed until the data is ready, at which point the data frame is expanded to include the data from the newly powered-up channel.



(1) In SPI protocol, the timing occurs on the falling edge of DRDY/FSYNC. Powering down all channels forces DRDY/FSYNC high.

Figure 5. Power-Down Timing

Table 8. Power-Down Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{PWDN}	PWDN pulse width to enter Power-Down mode	2			CLK periods
t_{NDR}	Time for new data ready (SPI)	129		130	Conversions ($1/f_{DATA}$)
t_{NDR}	Time for new data ready (Frame-Sync) (1)	128		129	Conversions ($1/f_{DATA}$)

(1) FSYNC clock running prior to the rising edge of PWDN. If PWDN is asynchronous to the FSYNC clock, t_{NDR-FS} varies from 127 to 128 conversions. If PWDN is made synchronous to FSYNC, then t_{NDR-FS} is stable.

FORMAT[2:0]

Data can be read from the MCA1274/78 with two interface protocols (SPI or Frame-Sync) and several options of data formats (TDM/Discrete and Fixed/Dynamic data positions). The FORMAT[2:0] inputs are used to select among the options. Table 9 lists the available options. See the *DOUT Modes* section for details of the DOUT Mode and Data Position.

Table 9. Data Output Format

FORMAT[2:0]	INTERFACE PROTOCOL	DOUT MODE	DATA POSITION
000	SPI	TDM	Dynamic
001	SPI	TDM	Fixed
010	SPI	Discrete	—
011	Frame-Sync	TDM	Dynamic
100	Frame-Sync	TDM	Fixed
101	Frame-Sync	Discrete	—
110	Modulator Mode	—	—

SERIAL INTERFACE PROTOCOLS

Data are retrieved from the MCA1274/78 using the serial interface. Two protocols are available: SPI and Frame-Sync. The same pins are used for both interfaces: SCLK, DRDY/FSYNC, DOUT[4:1] (DOUT[8:1] for MCA1278), and DIN. The FORMAT[2:0] pins select the desired interface protocol.

SPI SERIAL INTERFACE

The SPI-compatible format is a read-only interface. Data ready for retrieval are indicated by the falling DRDY output and are shifted out on the falling edge of SCLK, MSB first. The interface can be daisy-chained using the DIN input when using multiple devices.

NOTE: The SPI format is limited to a CLK input frequency of 27MHz, maximum. For CLK input operation above 27MHz (High-Speed mode only), use Frame-Sync format.

SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. The device shifts data out on the falling edge and the user normally shifts this data in on the rising edge.

Even though the SCLK input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data.

SCLK may be run as fast as the CLK frequency. SCLK may be either in free-running or stop-clock operation between conversions. Note that one f_{CLK} is required after the falling edge of DRDY until the first rising edge of SCLK. For best performance, limit f_{SCLK}/f_{CLK} to ratios of 1, 1/2, 1/4, 1/8, etc. When the device is configured for modulator output, SCLK becomes the modulator clock output.

DRDY/FSYNC (SPI Format)

In the SPI format, this pin functions as the DRDY output. It goes low when data are ready for retrieval and then returns high on the falling edge of the first subsequent SCLK. If data are not retrieved (that is, SCLK is held low), DRDY pulses high just before the next conversion data are ready, as shown in Figure 5. The new data are loaded within one CLK cycle before DRDY goes low. All data must be shifted out before this time to avoid being overwritten.

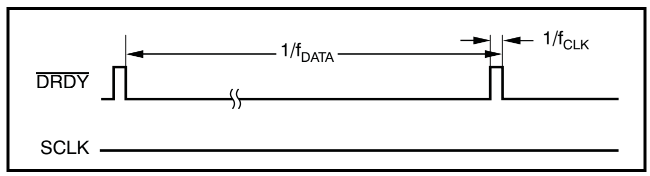


Figure 6. DRDY Timing with No Readback

DOUT

The conversion data are output on DOUT[4:1]/[8:1]. The MSB data are valid on DOUT[4:1]/[8:1] after DRDY goes low. Subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT after all channel data have been shifted out. When the device is configured for modulator output, DOUT[4:1]/[8:1] becomes the modulator data output for each channel .

DIN

This input is used when multiple MCA1274/78s are to be daisy-chained together. The DOUT1 pin of the first device connects to the DIN pin of the next, etc . It can be used with either the SPI or Frame-Sync formats.Data are shifted in on the falling edge of SCLK. When using only one MCA1274/78, tie DIN low.

FRAME-SYNC SERIAL INTERFACE

Frame-Sync format is similar to the interface often used on audio ADCs. It operates in slave fashion—the user must supply framing signal FSYNC (similar to the *left/right clock* on stereo audio ADCs) and the serial clock SCLK (similar to the *bit clock* on audio ADCs). The data are output MSB first or *left-justified* on the rising edge of FSYNC. When using Frame-Sync format, the FSYNC and SCLK inputs must be continuously running with the relationships shown in the Frame-Sync Timing Requirements.

SCLK

The serial clock (SCLK) features a Schmitt-triggered input and shifts out data on DOUT on the falling edge. It also shifts in data on the falling edge on DIN when this pin is being used for daisy-chaining. Even though SCLK has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. When using Frame-Sync format, SCLK must run continuously. If it is shut down, the data readback will be corrupted. The number of SCLKs within a frame period (FSYNC clock) can be any power-of-2 ratio of CLK cycles (1, 1/2, 1/4, etc), as long as the number of cycles is sufficient to shift the data output from all channels within one frame. When the device is configured for modulator output, SCLK becomes the modulator clock output .

DRDY/FSYNC (Frame-Sync Format)

In Frame-Sync format, this pin is used as the FSYNC input. The frame-sync input (FSYNC) sets the frame period, which must be the same as the data rate. The required number of f_{CLK} cycles to each FSYNC period depends on the mode selection and the CLKDIV input. Table 5 indicates the number of CLK cycles to each frame (f_{CLK}/f_{DATA}). If the FSYNC period is not the proper value, data readback will be corrupted.

DOUT

The conversion data are shifted out on DOUT[4:1]/[8:1]. The MSB data become valid on DOUT[4:1]/[8:1] after FSYNC goes high. The subsequent bits are shifted out with each falling edge of SCLK. If daisy-chaining, the data shifted in using DIN appear on DOUT[4:1]/[8:1] after all channel data have been shifted out. When the device is configured for modulator output, DOUT becomes the modulator data output .

DIN

This input isused when multiple MCA1274/78s are to be daisy-chained together.It can be used with either SPI or Frame-Sync formats. Data are shifted in on the falling edge of SCLK. When using only one MCA1274 /78, tie DIN low.

DOUT MODES

For both SPI and Frame-Sync interface protocols, the data are shifted out either through individual channel DOUT pins, in a parallel data format (Discrete mode), or the data for all channels are shifted out, in a serial format, through a common pin, DOUT1 (TDM mode).

TDM Mode

In TDM (time-division multiplexed) data output mode, the data for all channels are shifted out, in sequence, on a single pin (DOUT1). As shown in Figure 7, the data from channel 1 are shifted out first, followed by channel 2 data, etc. After the data from the last channel are shifted out, the data from the DIN input follow. The DIN is used to daisy-chain the data output from an additional MCA1274/78 or other compatible device. Note that when all channels of the MCA1274/78 are disabled, the interface is disabled, rendering the DIN input disabled as well. When one or more channels of the device are powered down, the data format of the TDM mode can be fixed or dynamic.

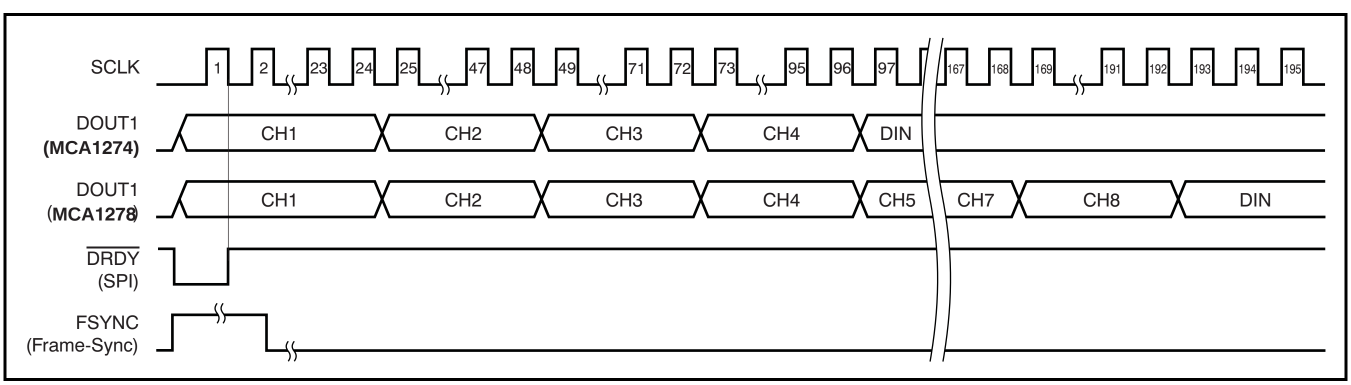


Figure 7. TDM Mode (All Channels Enabled)

TDM Mode, Fixed-Position Data

In this TDM data output mode, the data position of the channels remain fixed, regardless of whether the channels are powered down. If a channel is powered down, the data are forced to zero but occupy the same position within the data stream. Figure 8 shows the data stream with channel 1 and channel 3 powered down.

TDM Mode, Dynamic Position Data

In this TDM data output mode, when a channel is powered down, the data from higher channels shift one position in the data stream to fill the vacated data slot. Figure 9 shows the data stream with channel 1 and channel 3 powered down.

Discrete Data Output Mode

In Discrete data output mode, the channel data are shifted out in parallel using individual channel data output pins DOUT[4:1]/[8:1]. After the 24th SCLK, the channel data are forced to zero. The data are also forced to zero for powered down channels. Figure 10 shows the discrete data output format.

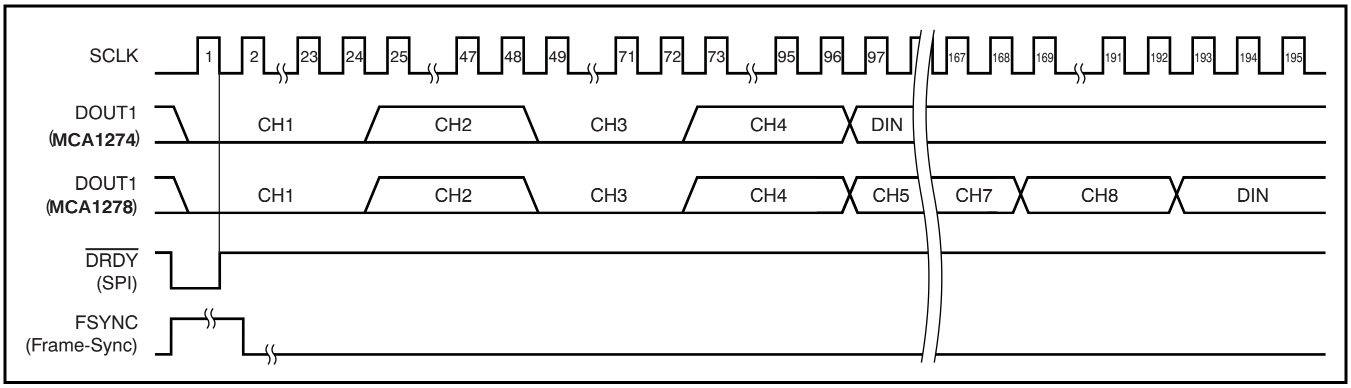


Figure 8. TDM Mode, Fixed-Position Data (Channels 1 and 3 Shown Powered Down)

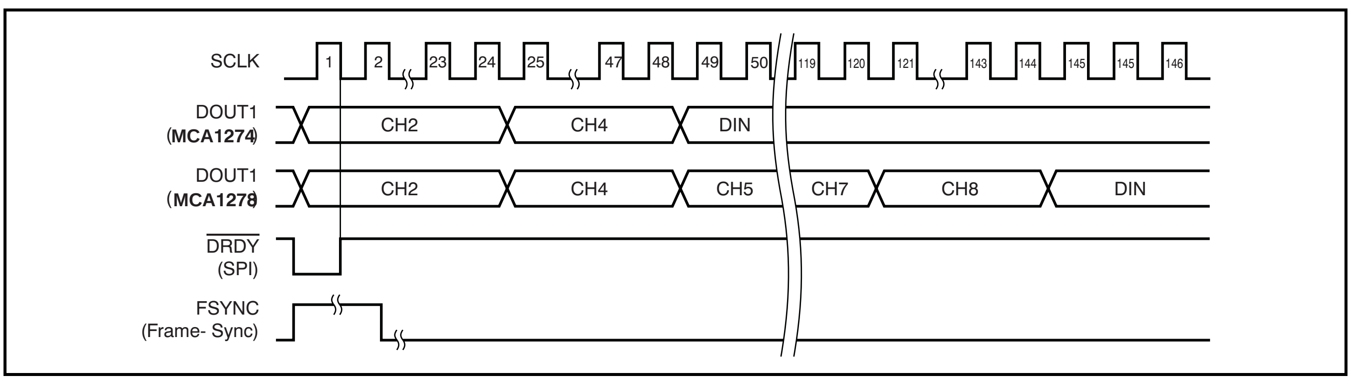


Figure 9. TDM Mode, Dynamic Position Data (Channels 1 and 3 Shown Powered Down)

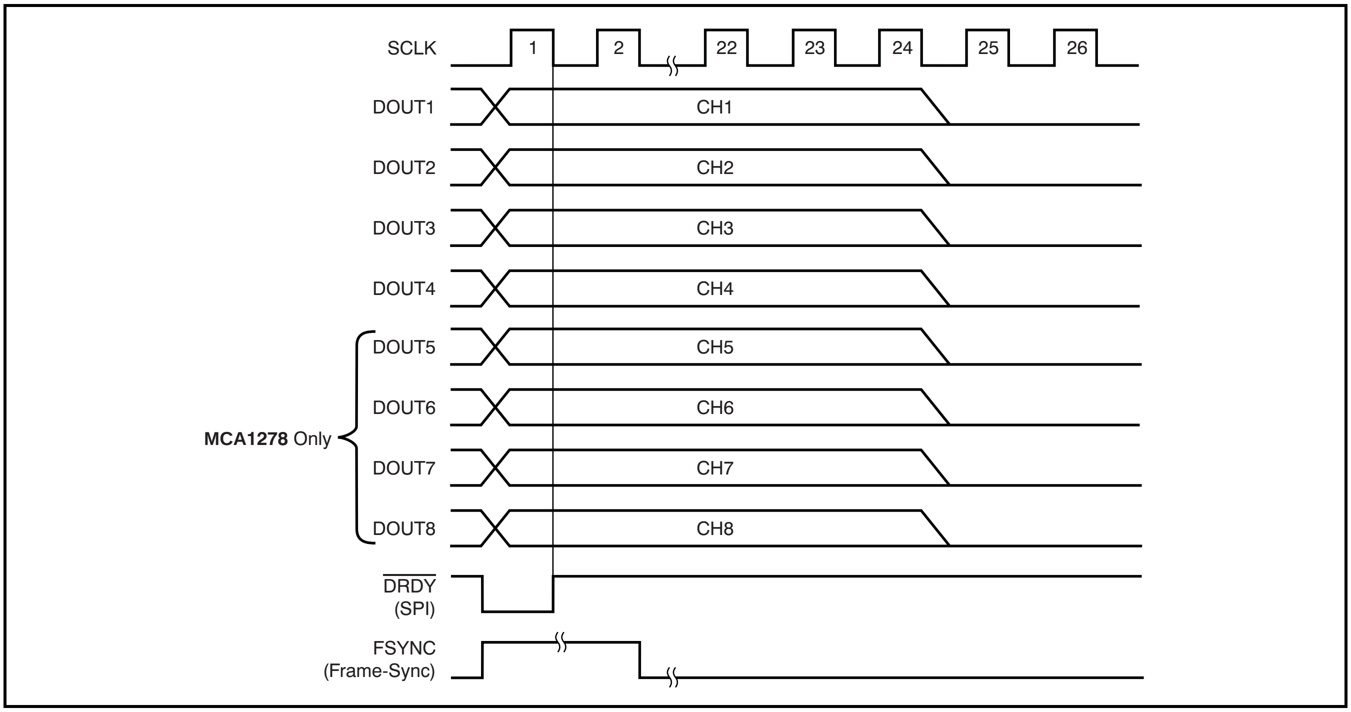


Figure 10. Discrete Data Output Mode

DAISY-CHAINING

Multiple MCA1274/78s can be daisy-chained together to output data on a single pin. The DOUT1 data output pin of one device is connected to the DIN of the next device. As shown in Figure 11, the DOUT1 pin of device 1 provides the output data to a controller, and the DIN of device 2 is grounded. Figure 12 shows the data format when reading back data.

The maximum number of channels that may be daisy-chained in this way is limited by the frequency of f_{SCLK}, the mode selection, and the CLKDIV input. The frequency of f_{SCLK} must be high enough to completely shift the data out from all channels within one f_{DATA} period. Table 10 lists the maximum number of daisy-chained channels when $f_{SCLK} = f_{CLK}$.

To increase the number of data channels possible in a chain, a segmented DOUT scheme may be used, producing two data streams. Figure 13 illustrates four MCA1274/78s, with pairs of MCA1274/78s daisy-chained together. The channel data of each daisy-chained pair are shifted out in parallel and received by the processor through independent data channels.

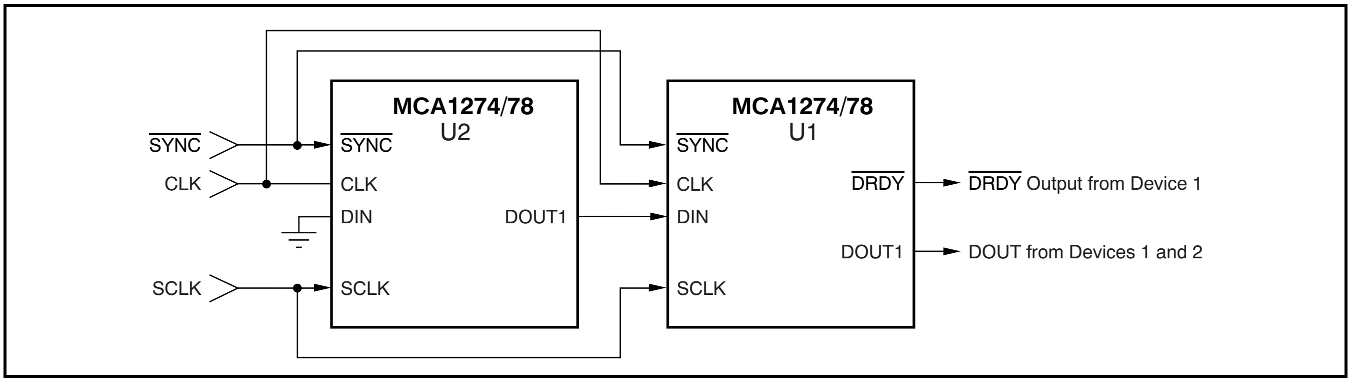
Table 10. Maximum Channels in a Daisy-Chain ($f_{SCLK} = f_{CLK}$)

MODE SELECTION	CLKDIV	MAXIMUM NUMBER OF CHANNELS
High-Speed	1	10
High-Resolution	1	21
Low-Power	1	21
	0	10
Low-Speed	1	106
	0	21

Whether the interface protocol is SPI or Frame-Sync, it is recommended to synchronize all devices by tying the SYNC inputs together. When synchronized in SPI protocol, it is only necessary to monitor the DRDY output of one MCA1274/78.

In Frame-Sync interface protocol, the data from all devices are ready after the rising edge of FSYNC.

Since DOUT1 and DIN are both shifted on the falling edge of SCLK, the propagation delay on DOUT1 creates a setup time on DIN. Minimize the skew in SCLK to avoid timing violations.



NOTE: The number of chained devices is limited by the SCLK rate and device mode.

Figure 11. Daisy-Chaining of Two Devices, SPI Protocol (FORMAT[2:0] = 000 or 001)

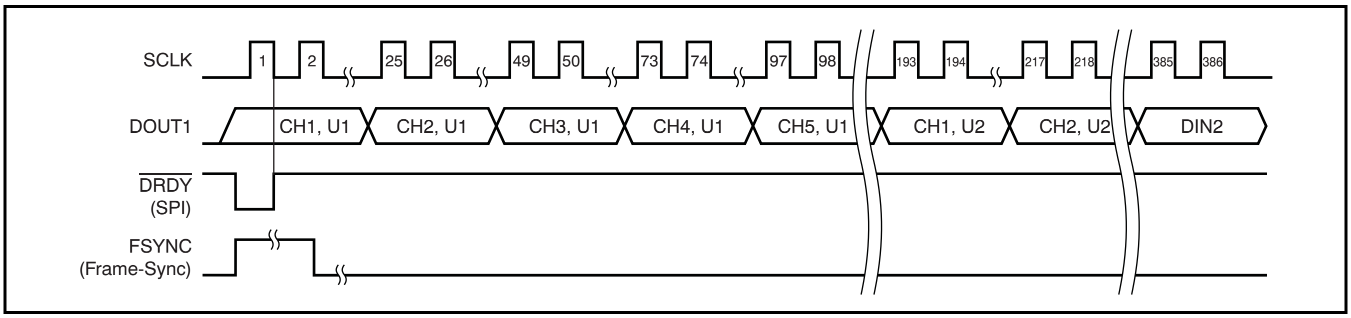


Figure 12. Daisy-Chain Data Format

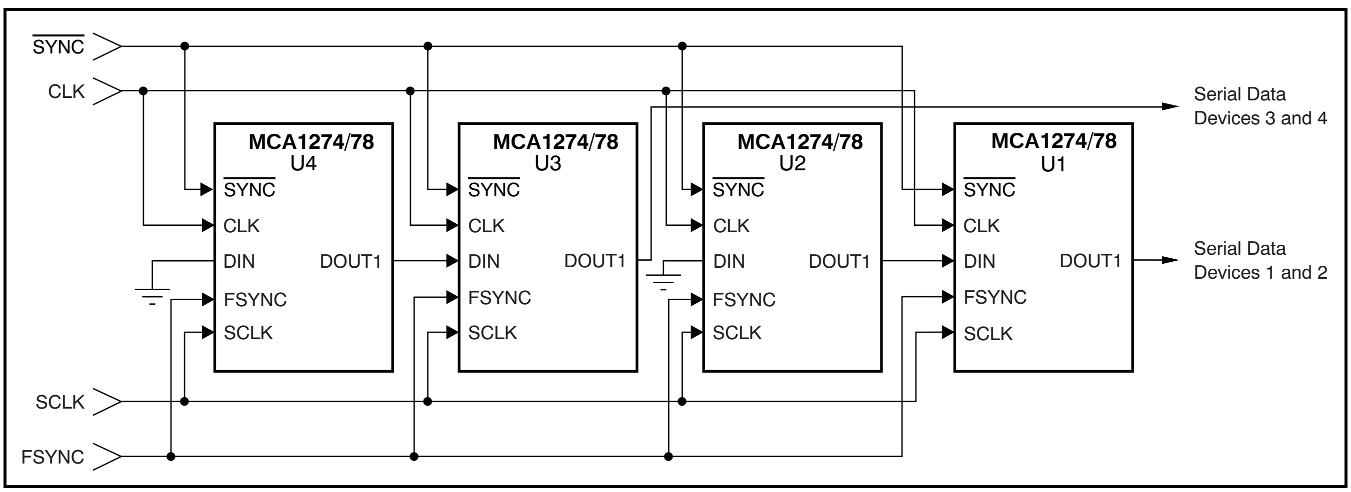
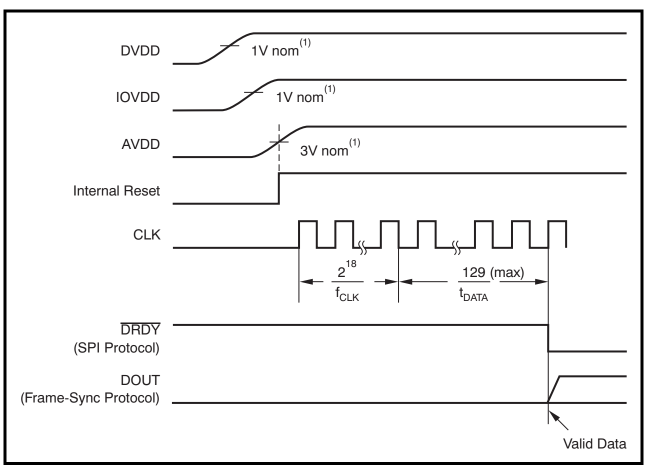


Figure 13. Segmented DOUT Daisy-Chain, Frame-Sync Protocol (FORMAT[2:0] = 011 or 100)

POWER SUPPLIES

The MCA1274/78 has three power supplies: AVDD ,DVDD, and IOVDD. AVDD is the analog supply that powers the modulator, DVDD is the digital supply that powers the digital core, and IOVDD is the digital I/O power supply. The IOVDD and DVDD power supplies can be tied together if desired (+1.8V). To achieve rated performance, it is critical that the power supplies are bypassed with 0.1μF and 10μF capacitors placed as close as possible to the supply pins. A single 10μF ceramic capacitor may be substituted in place of the two capacitors.

Figure 14 shows the start-up sequence of the MCA1274/78. At power-on, bring up the DVDD supply first, followed by IOVDD and then AVDD. Check the power-supply sequence for proper order, including the ramp rate of each supply. DVDD and IOVDD may be sequenced at the same time (for example, if the supplies are tied together). Each supply has an internal reset circuit whose outputs are summed together to generate a global power-on reset. After the supplies have exceeded the reset thresholds, 2^{18} f_{CLK} cycles are counted before the converter initiates the conversion process. Following the CLK cycles, the data for 129 conversions are suppressed by the MCA1274/78 to allow output of fully-settled data. In SPI protocol, DRDY is held high during this interval. In frame-sync protocol, DOUT is forced to zero. The power supplies should be applied before any analog or digital pin is driven. For consistent performance, assert SYNC after device power-on when data first appear.



(1) The power-supply reset thresholds are approximate.

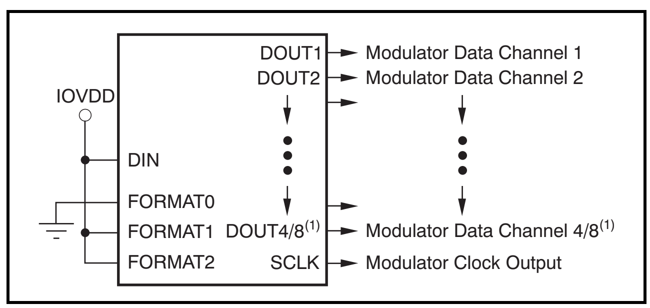
Figure 14. Start-Up Sequence

MODULATOR OUTPUT

The MCA1274/78 incorporates a 6th-order, single-bit, chopper-stabilized modulator followed by a multi-stage digital filter that yields the conversion results. The data stream output of the modulator is available directly, bypassing the internal digital filter. The digital filter is disabled, reducing the DVDD current, as shown in Table 11. In this mode, an external digital filter implemented in an ASIC, FPGA, or similar device is required. To invoke the modulator output, tie FORMAT[2:0], as shown in Figure 15. DOUT[4:1]/[8:1] then becomes the modulator data stream outputs for each channel and SCLK becomes the modulator clock output. The DRDY/FSYNC pin becomes an unused output and can be ignored. The normal operation of the Frame-Sync and SPI interfaces is disabled, and the functionality of SCLK changes from an input to an output, as shown in Figure 15.

Table 11. Modulator Output Clock Frequencies

MODE [1:0]	CLKDIV	MODULATOR CLOCK OUTPUT (SCLK)	MCA1274 DVDD (mA)	MCA1278 DVDD (mA)
00	1	$f_{CLK}/4$	4.5	8
01	1	$f_{CLK}/4$	4.0	7
10	1	$f_{CLK}/8$	2.5	4
	0	$f_{CLK}/4$	2.5	4
11	1	$f_{CLK}/40$	1.0	1
	0	$f_{CLK}/8$	0.5	1



(1) The MCA1274 has four channels; the MCA1278 has eight channels.

Figure 15. Modulator Output

In modulator output mode, the frequency of the modulator clock output (SCLK) depends on the mode selection of the MCA1274/78. Table 11 lists the modulator clock output frequency and DVDD current versus device mode.

Figure 16 shows the timing relationship of the modulator clock and data outputs.

The data output is a modulated 1s density data stream. When $V_{IN} = +V_{REF}$, the 1s density is approximately 80% and when $V_{IN} = -V_{REF}$, the 1s density is approximately 20%.

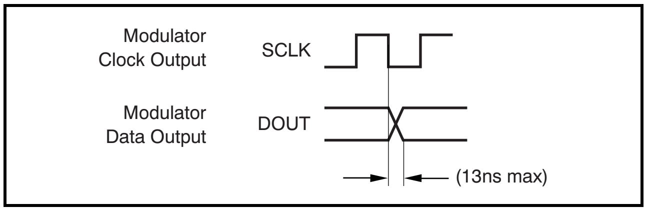


Figure 16. Modulator Output Timing

PIN TEST USING TEST[1:0] INPUTS

The test mode feature of the MCA1274 and MCA1278 allows continuity testing of the digital I/O pins. In this mode, the normal functions of the digital pins are disabled and routed to each other as pairs through internal logic, as shown in Table 12. The pins in the left column drive the output pins in the right column.

Note: some of the digital input pins become outputs; these outputs must be accommodated in the design. The analog input, power supply, and ground pins all remain connected as normal. The test mode is engaged by setting the pins TEST [1:0] = 11. For normal converter operation, set TEST[1:0] = 00. Do not use '01' or '10'.

Table 12. Test Mode Pin Map (TEST[1:0] = 11)

TEST MODE PIN MAP	
INPUT PINS	**OUTPUT PINS**
$\overline{\text{PWDN1}}$	DOUT1
$\overline{\text{PWDN2}}$	DOUT2
$\overline{\text{PWDN3}}$	DOUT3
$\overline{\text{PWDN4}}$	DOUT4
$\overline{\text{PWDN5}}$	DOUT5
$\overline{\text{PWDN6}}$	DOUT6
$\overline{\text{PWDN7}}$	DOUT7
$\overline{\text{PWDN8}}$	DOUT8
MODE0	DIN
MODE1	$\overline{\text{SYNC}}$
FORMAT0	CLKDIV
FORMAT1	FSYNC/$\overline{\text{DRDY}}$
FORMAT2	SCLK

VCOM OUTPUT

The VCOM pin provides a voltage output equal to AVDD/2. The intended use of this output is to set the output common-mode level of the analog input drivers. The drive capability of the output is limited; therefore, the output should only be used to drive high-impedance nodes (> 1MΩ). In some cases, an external buffer may be necessary. A 0.1μF bypass capacitor is recommended to reduce noise pickup.

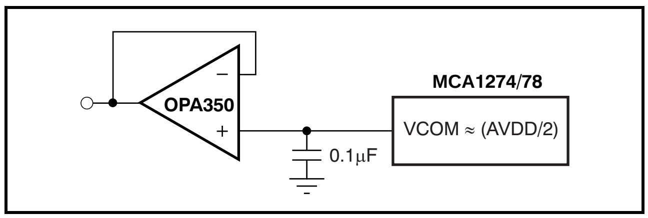


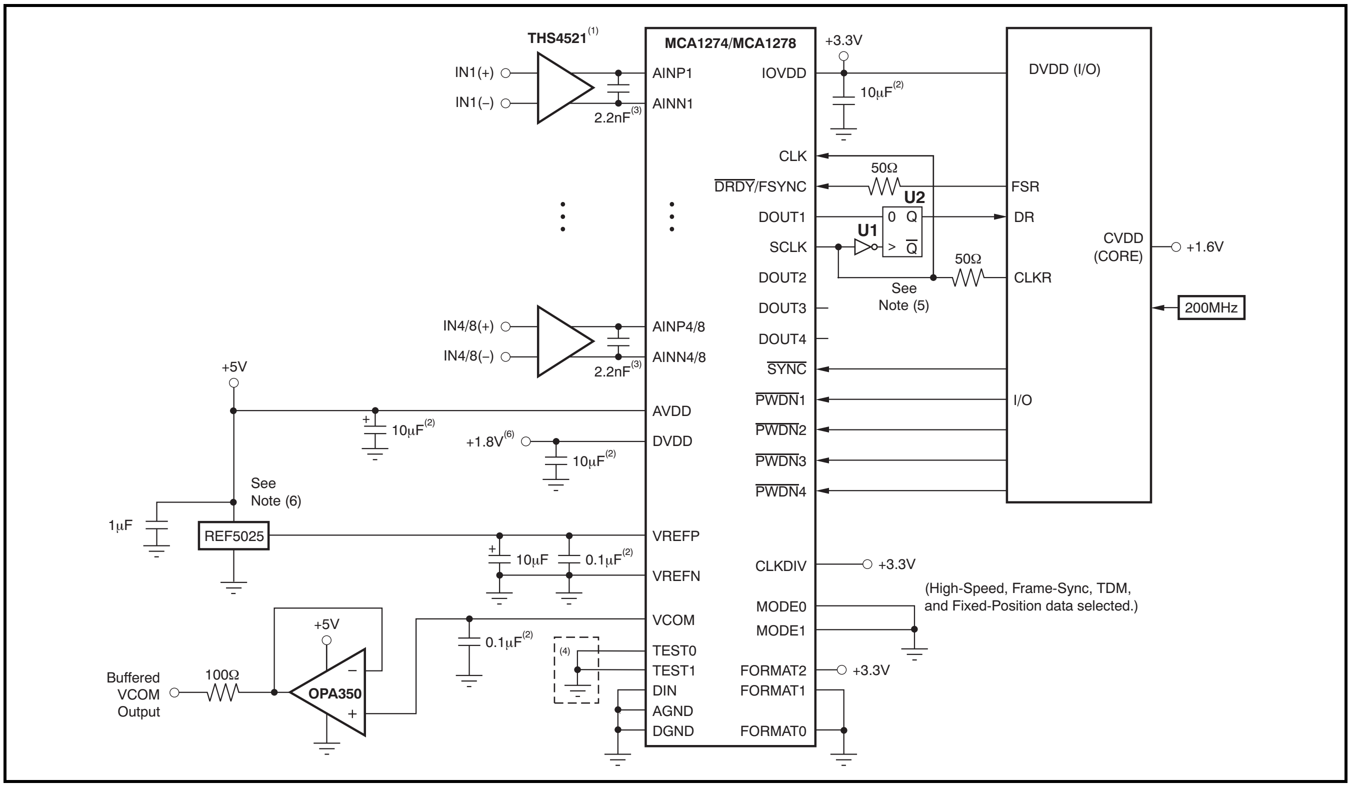
Figure 17. VCOM Output

APPLICATION INFORMATION

To obtain the specified performance from the MCA1274/78, the following layout and component guidelines should be considered.

1. **Power Supplies:** The device requires three power supplies for operation: DVDD, IOVDD, and AVDD. The allowed range for DVDD is 1.65V to 1.95V; the range of IOVDD is 1.65V to 3.6V; AVDD is restricted to 4.75V to 5.25V. For all supplies, use a 10μF tantalum capacitor, bypassed with a 0.1μF ceramic capacitor, placed close to the device pins. Alternatively, a single 10μF ceramic capacitor can be used. The supplies should be relatively free of noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power-supply source is used, the voltage ripple should be low (less than 2mV) and the switching frequency outside the passband of the converter.
2. **Ground Plane:** A single ground plane connecting both AGND and DGND pins can be used. If separate digital and analog grounds are used, connect the grounds together at the converter.
3. **Digital Inputs:** It is recommended to source-terminate the digital inputs to the device with 50Ω series resistors. The resistors should be placed close to the driving end of digital source (oscillator, logic gates, DSP, etc.) This placement helps to reduce ringing on the digital lines (ringing may lead to degraded ADC performance).
4. **Analog/Digital Circuits:** Place analog circuitry (input buffer, reference) and associated tracks together, keeping them away from digital circuitry (DSP, microcontroller, logic). Avoid crossing digital tracks across analog tracks to reduce noise coupling and crosstalk.
5. **Reference Inputs:** It is recommended to use a minimum 10μF tantalum with a 0.1μF ceramic capacitor directly across the reference inputs, VREFP and VREFN. The reference input should be driven by a low-impedance source. For best performance, the reference should have less than $3\mu V_{RMS}$ in-band noise. For references with noise higher than this level, external reference filtering may be necessary.
6. **Analog Inputs:** The analog input pins must be driven differentially to achieve specified performance. A true differential driver or transformer (ac applications) can be used for this purpose. Route the analog inputs tracks (AINP, AINN) as a pair from the buffer to the converter using short, direct tracks and away from digital tracks. A 1nF to 10nF capacitor should be used directly across the analog input pins, AINP and AINN. A low-k dielectric (such as COG or film type) should be used to maintain low THD. Capacitors from each analog input to ground can be used. They should be no larger than 1/10 the size of the difference capacitor (typically 100pF) to preserve the ac common-mode performance.
7. **Component Placement:** Place the power supply, analog input, and reference input bypass capacitors as close as possible to the device pins. This layout is particularly important for small-value ceramic capacitors. Larger (bulk) decoupling capacitors can be located farther from the device than the smaller ceramic capacitors.

Figure 8 to Figure 20 illustrate basic connections and interfaces that can be used with the MCA1274.



(1) External Schottky clamp diodes or series resistors may be needed to prevent overvoltage on the inputs. Place the THS4521 drivers close to the MCA1278 inputs.

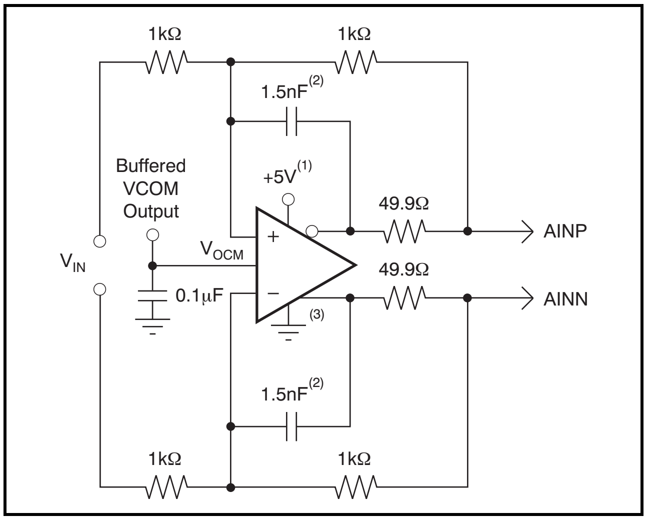
(2) Indicates ceramic capacitors.

(3) Indicates COG ceramic capacitors.

(4) Optional. For pin test mode.

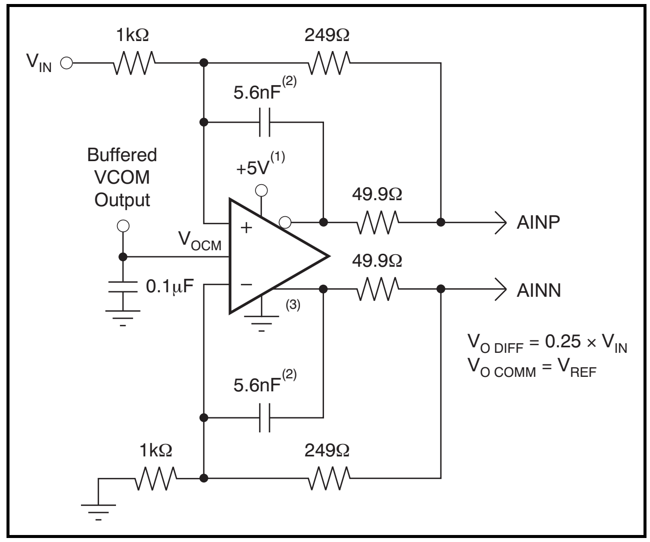
(5) These components re-timer the data output of MCA1274/MCA1278 to interface with the DSP.

Figure 18. MCA1274 Basic Connection Drawing



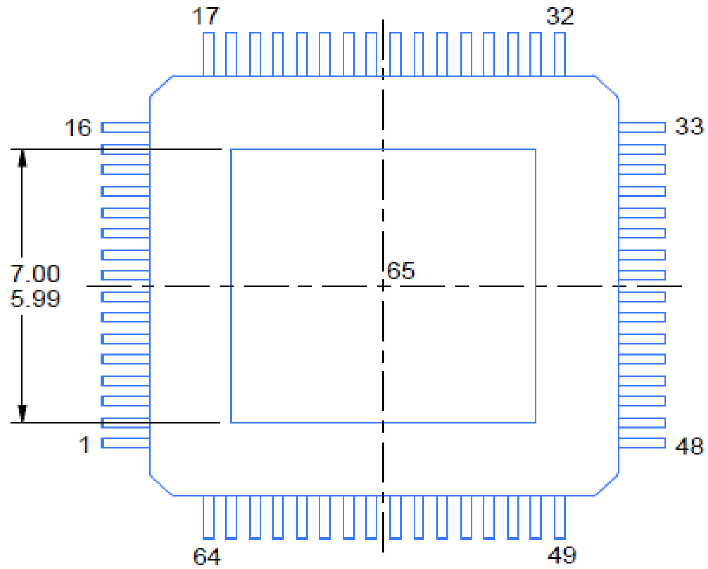
(1) Bypass with 10μF and 0.1μF capacitors.
(2) 2.7nF for Low-Power mode; 15nF for Low-Speed mode.
(3) Alternate driver OPA1632 (using ±12V supplies).

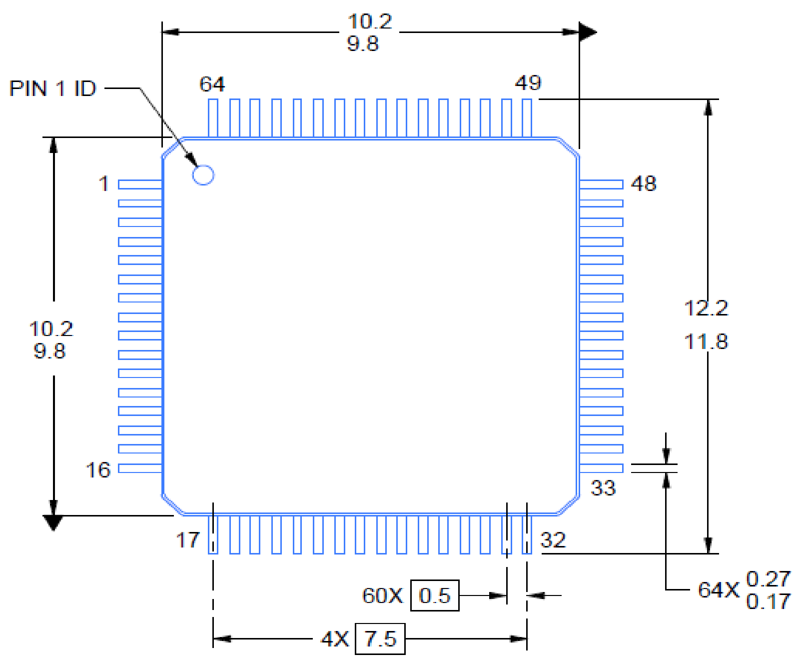
Figure 19. Basic Differential Input Signal Interface



(1) Bypass with 10μF and 0.1μF capacitors.
(2) 10nF for Low-Power mode; 56nF for Low-Speed mode.
(3) Alternate driver OPA1632 (using ±12V supplies).

Figure 20. Basic Single-Ended Input Signal Interface





ORDERING GUIDE

Model	Description	Temperature Range	Package	Carrier	ROHS
MCA1274CFP-H	4-channel high-temp synchronous acquisition ADC	–55°C ~ +210°C	64-CQFP	160/Tray	Y
MCA1278CFP-H	8-channel high-temp synchronous acquisition ADC	–55°C ~ +210°C	64-CQFP	160/Tray	Y
MCA1274TFP-H	4-channel high-temp synchronous acquisition ADC	–55°C ~ +175°C	64-eTQFP	160/Tray	Y
MCA1278TFP-H	8-channel high-temp synchronous acquisition ADC	–55°C ~ +175°C	64-eTQFP	160/Tray	Y
MCA1278TFP-M	8-channel high-temp synchronous acquisition ADC	–55°C ~ +125°C	64-eTQFP	160/Tray	Y
MCA1274TFP-M	4-channel high-temp synchronous acquisition ADC	–55°C ~ +125°C	64-eTQFP	160/Tray	Y