18-Bit, 5 MSPS PulSAR Differential ADC

Data Sheet

MCA7960

FEATURES

- Throughput: 5 MSPS
- 18-bit resolution with no missing codes
- Excellent ac and dc performance(Typical)
  - Dynamic range: 100 dB
  - SNR: 99 dB
  - THD: –117 dB
- SFDR: 115dB
- INL: ±2 LSB (maximum)
- DNL: ±0.99 LSB (maximum)
- Allow ±VREF(0V to +VREF V)any input range
- maximum VREF 5V ,Typical :4.096 V - 5 V
- Low power dissipation：64.5 mW
- Supply Voltage:1.8V/5V
- SAR architecture：No latency/pipeline delay
- Logical Digital Interface: 1.8V
- Serial LVDS interface
- Operating temperature range of –40°C to +85°C
- QFN-32Lead Packege

APPLICATIONS

- Digital imaging systems
  - Digital X-rays
  - Computed tomography
  - IR cameras
  - MRI gradient control
- High speed data acquisition
- Spectroscopy
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

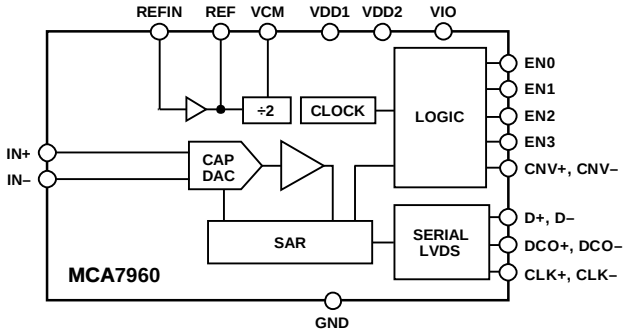


Figure 1.

GENERAL DESCRIPTION

The MCA7960 is an 18-bit,5 MSPS,charge redistribution successive approximation (SAR), analog-to-digital converter (ADC). The SAR architecture allows unmatched performance both in noise and in linearity.The MCA7606 contains a low power,high speed,18-bit sampling ADC,an internal conversion clock,and a internal reference buffer.On the CNV± edge,the MCA7960 samples the voltage differenve between the IN+ and IN- pins.The voltage on these pins swing in opposite phase between 0V and 4.096Vand between 0V and 5V.The reference voltage is applied to the part axternally.All conversion results are available on a signle LVDS self clocked or echoed clock serial interface.The MCA7960 is available in a 32-lead QFN with operation specified from -40°C to +85°C.

SPECIFICATIONS

Table 1.

VDD1 = 5 V; VDD2 = 1.8 V; VIO = 1.8 V; all specifications T = 25°C, unless otherwise noted.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION	VDD1=5V,VDD2=1.8V,VIO=1.8V		18		Bits
Power VDD1 Current	EN0-EN3=1001,REFIN=0		0.9	2.0	mA
Power VDD2 Current	EN0-EN3=1001,REFIN=0		7.8	15	mA
Power VIO Current	EN0-EN3=1001,REFIN=0		9.0	15	mA
Power Dissipation	EN0-EN3=1001,REFIN=0		35	75	mW
No Missing Code	fIN=1kHz,VREF=5V		18		Bits
INL	fIN=1KHz,VREF=5V	-6.0	+1.5/-1.5	+6.0	LSB
DNL	fIN=1KHz,VEREF=5V	-0.99	+0.85/-0.60	+1.75	LSB
Transition Noise	fIN=DC,VREF=5V		1.25	5.0	LSB
Offset Error		-25	+1.00	+25	LSB
Offset Drift	fIN=DC,VREF=5V	-8	+0.20	+8	ppm/°C
Gain Error		-50	-10	+50	LSB
Gain Drift	fIN=DC,VREF=5V	-16	+0.20	+16	ppm/°C
Digital Input Voltage High Level, VIH		1.5	1.5		V
Digital Input Voltage Low Level, VIL	VDD1=5V,VDD2=1.8V,VIO=1.8V		0.3	0.3	V
Dynamic Range	fIN=DC,VREF=5V	94	97.5		dB
	fIN=DC,VREF=4.096V	93	96.0		dB
SNR	fIN=1KHz,VREF=5V	93	95.5		dB
	fIN=1KHz,VREF=4.096V	92	95.0		dB
ENOB	fIN=1KHz,VREF=5V	14.9	15.70		bits
	fIN=1KHz,VREF=4.096V	14.8	15.60		bits
SINAD	fIN=1KHz,VREF=5V	92	95.0		dB
	fIN=1KHz,VREF=4.096V	91.5	94.5		dB
SFDR	fIN=1KHz,VREF=5V	105	115.0		dB
	fIN=1KHz,VREF=4.096V	101	107.0		dB
THD	fIN=1KHz,VREF=5V		-113.0	-101	dB
	fIN=1KHz,VREF=4.096V		-108.0	-98	dB
Sampling Rate	fIN=1KHz,VREF=5V			5	MSPS
Conversion Time Interval	fIN=1KHz,VREF=5V	200	200		ns
CNV High Plus Width	fIN=1KHz,VREF=5V	10	20	120	ns
Output Data Sampling Rate	fIN=1KHz,VREF=5V	150	100	250	MHz
Delay from CLK to DCO	VDD1=5V,VDD2=1.8V,VIO=1.8V	0	2.8	10	ns

ÿ maximum values are guaranteed by characterization.
Using an external reference.

TIMING SPECIFICATIONS

VDD1 = 5 V; VDD2 = 1.8 V; VIO = 1.71 V to 1.89 V; REF = 5 V or 4.096 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
Time Between Conversions	t_{CYC}	200			ns
Acquisition Time	t_{ACQ}		t_{CYC} − 115		ns
CNV± High Time	t_{CNVH}	10		0.6 × t_{CYC}	ns
CNV± to D± (MSB) Ready	t_{MSB}			200	ns
CNV± to Last CLK± (LSB) Delay	t_{CLKL}			160	ns
CLK± Period[1]	t_{CLK}	3.33	4	(t_{CYC} − t_{MSB} + t_{CLKL})/n	ns
CLK± Frequency	f_{CLK}		250	300	MHz
CLK± to DCO± Delay (Echoed Clock Mode)	t_{DCO}	0	3	5	ns
DCO± to D± Delay (Echoed Clock Mode)	t_D		0	1	ns
CLK± to D± Delay	t_{CLKD}	0	3	5	ns

[1] For the maximum CLK± period, the window available to read data is t_{CYC} − t_{MSB} + t_{CLKL}. Divide this time by the number of bits (n) to be read, giving the maximum CLK± frequency that can be used for a given conversion CNV± frequency. In echoed clock interface mode, n = 18; in self clocked interface mode, n = 20.

Timing Diagrams

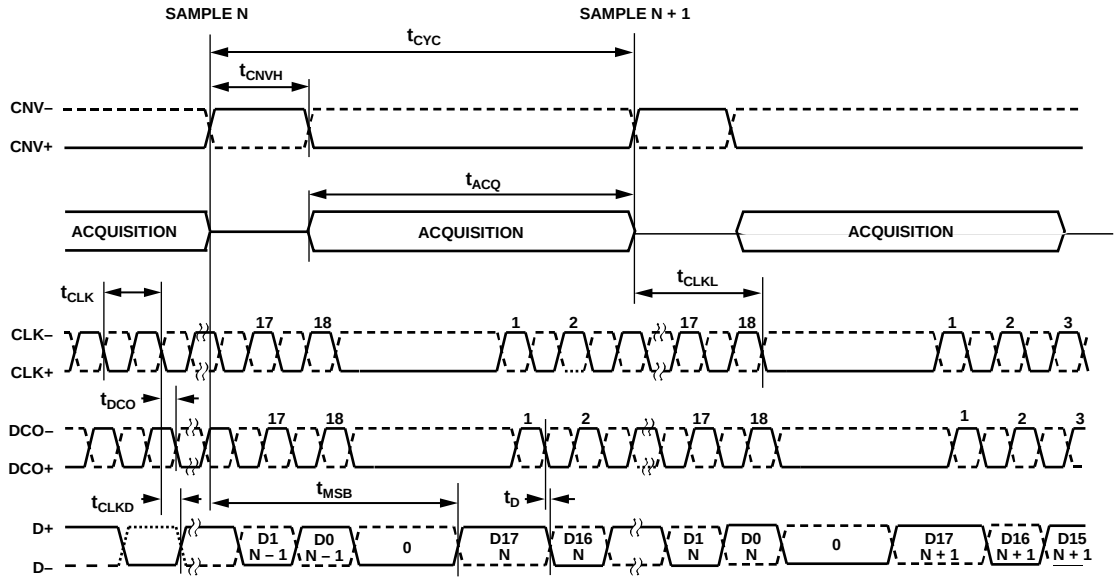


Figure 2. Echoed Clock Interface Mode Timing Diagram

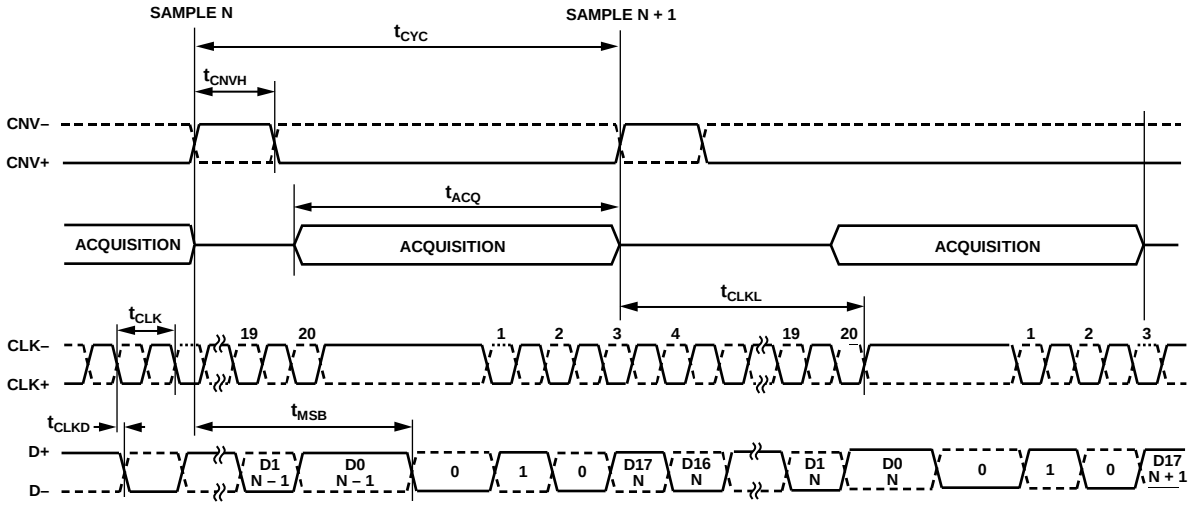


Figure 3. Self Clocked Interface Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Analog Inputs/Outputs	
IN+, IN– to GND	–0.3 V to REF +0.3V
REF[1] to GND	–0.3 V to +6 V
VCM to GND	–0.3 V to +6 V
REFIN to GND	–0.3 V to +6 V
Supply Voltages	
VDD1	–0.3 V to +6 V
VDD2, VIO	–0.3 V to +2.1 V
Digital Inputs to GND	–0.3 V to VIO + 0.3 V
Digital Outputs to GND	–0.3 V to VIO + 0.3 V
Input Current to Any Pin Except Supplies	±10 mA
Operating Temperature Range (Commercial)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
ESD Ratings	
Human Body Model	4 kV
Machine Model	200 V
Field-Induced Charged-Device Model	1.25 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

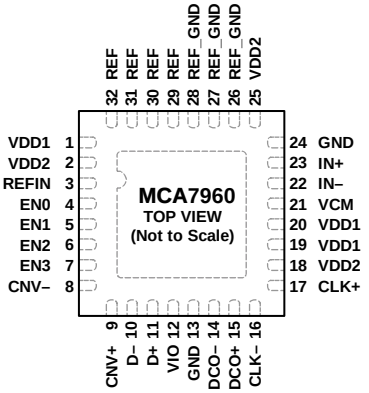
Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP_VQ	40	4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. CONNECT THE EXPOSED PAD TO THE GROUND PLANE OF THE PCB USING MULTIPLE VIAS.

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 19, 20	VDD1	P	Analog 5 V Supply. Decouple the 5 V supply with a 100 nF capacitor.
2, 18, 25	VDD2	P	Analog 1.8 V Supply. Decouple this pin with a 100 nF capacitor.
12	VIO	P	Input/Output Interface Supply. Use a 1.8 V supply and decouple this pin with a 100 nF capacitor.
13, 24	GND	P	Ground.
26, 27, 28	REF_GND	P	Reference Ground. Connect the capacitors on the REF pin between REF and REF_GND. Tie REF_GND to GND.
3	REFIN	AI	Prebuffer Reference Voltage. It is driven with an external reference voltage of 2.048 V. When driving an external 2.048 V reference, a 100 nF capacitor is required. If using an external 5 V or 4.096 V reference (connected to REF), connect this pin to ground.
4, 5, 6, 7	EN0, EN1, EN2,[2] EN3	DI	Enable.[2] The logic levels of these pins set the operation of the device, as described in Table 8.
8, 9	CNV–, CNV+	DI	Convert Input. These pins act as the conversion control pin. On the rising edge of these pins, the analog inputs are sampled and a conversion cycle is initiated. CNV+ works as a CMOS input when CNV– is grounded; otherwise, CNV+ and CNV– are differential LVDS inputs.
10, 11	D–, D+	DO	LVDS Data Outputs. The conversion data is output serially on these pins.
14, 15	DCO–, DCO+	DO	LVDS Buffered Clock Outputs. When DCO+ is grounded, the self clocked interface mode is selected. In this mode, the 18-bit results on D± are preceded by an initial 0 (which is output at the end of the previous conversion), followed by a 2-bit header (10) to allow synchronization of the data by the digital host with extra logic. The 1 in this header provides the reference to acquire the subsequent conversion result correctly. When DCO+ is not grounded, the echoed clock interface mode is selected. In this mode, DCO± is a copy of CLK±. The data bits are output on the falling edge of DCO+ and can be captured in the digital host on the next rising edge of DCO+.
16, 17	CLK–, CLK+	DI	LVDS Clock Inputs. This clock shifts out the conversion results on the falling edge of CLK+.
21	VCM	AO	Common-Mode Output. When using any reference scheme, this pin produces one-half the voltage present on the REF pin, which can be useful for driving the common mode of the input amplifiers.
22	IN–	AI	Differential Negative Analog Input. Referenced to and must be driven 180° out of phase with IN+.
23	IN+	AI	Differential Positive Analog Input. Referenced to and must be driven 180° out of phase with IN–.
29, 30, 31, 32	REF	AI/O	Buffered Reference Voltage. When using the 2.048 V external reference (REFIN input), the 4.096 V system reference is produced at this pin. When using an external reference of 4.096 V or 5 V on this pin, the internal reference buffer must be disabled. Connect the REF pins with the shortest trace possible to a single 10 µF, low ESR, low ESL capacitor. The other side of the capacitor must be placed close to GND.
33	EP		Exposed Pad. The exposed pad is located on the underside of the package. Connect the exposed pad to the ground plane of the PCB using multiple vias.

[1] AI = analog input; AI/O = bidirectional analog; AO = analog output; DI = digital input; DO = digital output; P = power.
[2] EN2 = 0 sets the 28 MHz of input bandwidth, and EN2 = 1 sets the 9 MHz of input bandwidth. EN3 = 1 enables the V_{CM} reference output.

OUTLINE DIMENSIONS

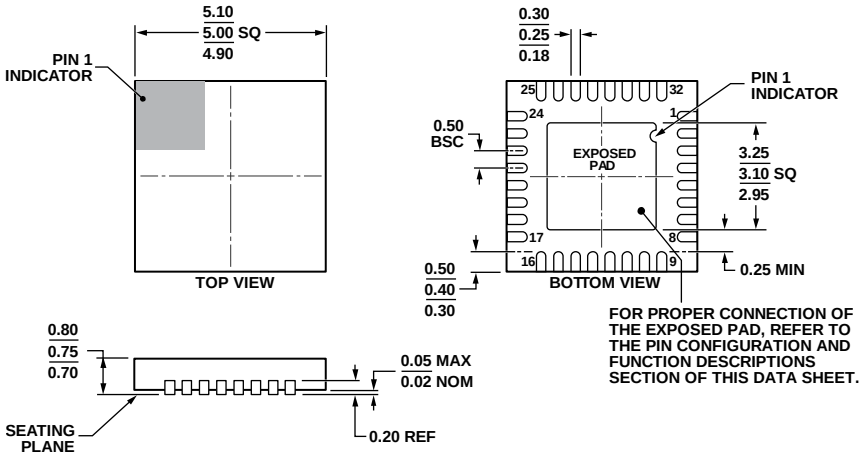


Figure 4.
5 mm × 5 mm Body
QFN-32Lead
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
MCA7960	–40°C to +85°C	32-Lead QFN	Tray-490

[1] Z = RoHS Compliant Part.