Dual, 16-Bit, 250MSPS,1.8V Analog-to-Digital Converter

Data Sheet

MCA42LB69-250

FEATURES

1.8 V supply operation
Low power: 600 mW per channel at 250MSPS
SNR = 74dBFs @f IN up to 70MHz@250MSPS(-1dBFs)
SFDR = - 90 dBFs@fIN up to 70MHz@250MSPS(-1dBFs)
Maximum Clock Rate:250MSPS
DDR LVDS Interface
800 MHz full power analog bandwidth
Pin-compatible with ADS42LB69
With internal dither

APPLICATIONS

Communication and cable infrastructure
Multi-carrier ,multi-mode cellular receiver
Radar and smart antenna arrays
Broadband wireless
Quadrature radio receivers
Diversity radio receivers
Test equipment
Microwave and I/O receivers
Repeaters
Power amplifier linearization

GENERAL DESCRIPTION

The MCA42LB69-250 is a dual, 16-bit, 250 MSPS analog-to-digital converter (ADC) optimized for high performance , low power,and ease of use. The product operates at a conversion rate of up to 250 MSPS and is optimized for outstanding dynamic performance in wideband carrier and broadband systems.All necessary functions,inculding a track-and -hold(T/H)and voltage reference ,are inculded on the chip to provide a complete signal conversion solution.

Fabricated on an advanced CMOS process,the MCA42LB69-250 is available in a 64-lead VQFN package,specified over the Military temperature range (-55°C to +125°C)

FUNCTIONAL BLOCK DIAGRAM

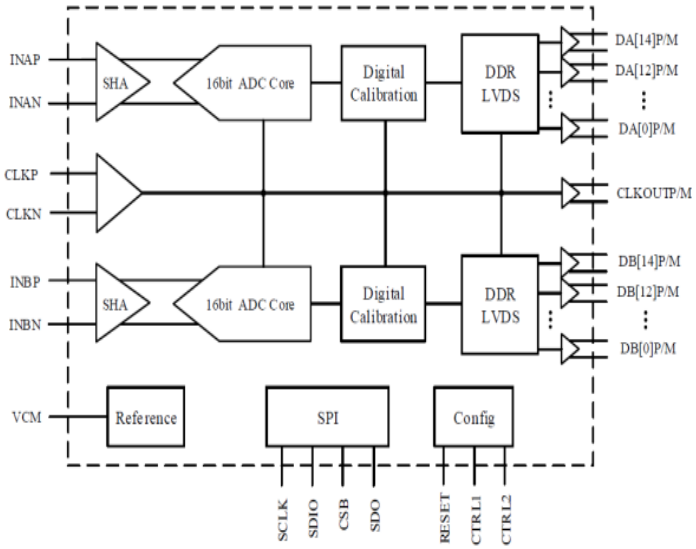

Figure 1.

PRODUCT HIGHLIGHTS

1. High Performance --Maintains 74dBFS SNR @250MSPS with a 70MHz input.
2. Low Power --Consumes only 600mW @250MSPS.
3. Ease of use --LVDS output data and output clocks signal allow interface to current FPGA techology.The on-chip reference and sample and hold provide flexibilty in system design .
4. Serial Port Control--Standard serial port interface suppo -rts various product functions ,such as data formatting , disabling the clock duty cycle stabilizer ,power -down , gain adjust,and output test pattern generation .
5. Pin-Compatible --Pin-Compatible with ADS42LB69

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V

Table 1.

Parameter	Min	Typ	Max	Unit
RESOLUTION		16		bit
CLOCK INPUT	10		250	MHz
ANALOG INPUT				
Input Bandwidth(2V input)		800		MHz
Differential Input Voltage (Vpp)		2		V
Input Common-mode Voltage		1		
ACCURACY				
Offset			±1	mV
Gain Error			±5	%FS
Differential Nonlinearity(DNL)			±0.5	LSB
Integral Nolinearity(INL)			±6	LSB
POWER SUPPLY				
AVDD	1.7	1.8	1.9	V
DRVDD	1.7	1.8	1.9	V
IAVDD analog supply current		800		mA
IDRVDD digital supply current		120		mA
POWER CONSUMPTION (per channel)		600		mW

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, Clock Duty Cycle=50%,AIN=-1dBFs,Sampling rate=250MSPS.

Table 2 .

Parameter		Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO(SNR)	f_{IN} = 10MHz		74.2		dBFS
	f_{IN} = 70MHz		74		dBFS
	f_{IN} = 225MHz	70.8	73.2		dBFS
SIGNAL-TO-NOISE-AND-DISTORITON RATIO(SNDR)	f_{IN} = 10MHz		74		dBFS
	f_{IN} = 70MHz		73.9		dBFS
	f_{IN} = 225MHz	69.6	71.5		dBFS
EFFECTIVE NUMBER OF BITS(ENOB)	f_{IN} = 10MHz		12		bits
	f_{IN} = 70MHz		12		bits
	IN = 225MHz	11.3	11.6		bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)	f_{IN} = 10MHz		89		dBFS
	f_{IN} = 70MHz		89.8		dBFS
	IN = 225MHz	72	75.5		dBFS
ANALOG INPUT BANDWIDTH			800		MHz
POWER SUPPLY REJECTION RATIO (PSRR)	For 50-mVPP signal on AVDD supply,up to10MHz	40			dB
CHANNEL ISOLATION			105		dB

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, unless otherwise noted.

Table 3 .

Parameter	Test Condition	Min	Typ	Max	Unit
LOGIC INPUT(RESET、SCLK、SDATA、SEN、CTRL1、CTRL2)					
V_{IH},Logic 1 Voltage		1.3			V
V_{IL},Logic 0 Voltage				0.4	V
I_{IH},Logic 1 Current	VHIGH=1.8V		10		uA
I_{IL},Low Level Input Current	VLOW=0V		0		uA
LOGIC OUTPUT(OCRA、OVRB、SDOUT)					
V_{OH},Logic 1 Voltage		DRVDD-0.1	DRVDD		V
V_{OL},Logic 1 Voltage			0	0.1	V
LVDS DIGITAL OUTPUT					
V_{ODH},High Level differential output voltage	External termination 100 Ω	250	350	500	mV
V_{ODL},Low Level differential output voltage	External termination 100 Ω	-500	-350	-250	mV
V_{COM},Input Common-mode voltage			1.05		V

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.1 V
DRVDD to AGND	−0.3 V to +2.1 V
Input Voltage	−0.3 V to +2.0 V
CLK+, CLK− to AGND	−0.3 V to AVDD+2.0 V
VIN+x, VIN−x to AGND	−0.3 V to AVDD+2.0 V
SCLK,SEN,SDATA,RESET,CTRL1,CTRL2	−0.3 V to +2.1 V
Environmental	
Operating Temperature Range	-55°C to 150°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5. ESD Level

		Max	Unit
$V_{(ESD)}$Electrostatic discharge	HBM,MIL-STD-883K/ Method3015.9	±2500	V
$V_{(ESD)}$Electrostatic discharge	CDM,ESDA/JEDEC JS-002-2018	±1000	V

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

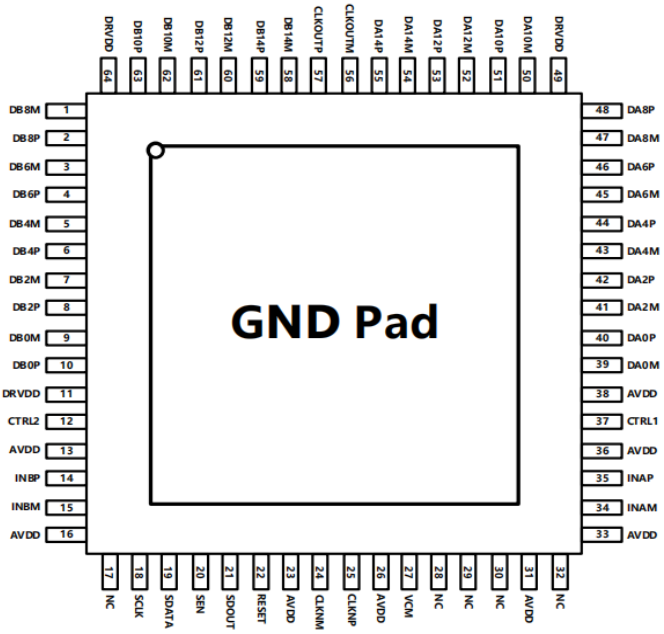

Figure 2 . 64-Lead VQFN Pin Configuration, Top View

Table 6 . Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
34,35	INAM,INAP	Channel A Differential Analog Input
14,15	INBP,INBM	Channel B Differential Analog Input
27	VCM	Common-mode Voltage for Analog Input,1.0V
24,25	CLKINP, CLKINM	Differential clock input for ADC(with an internal common mode bias0.95V)
17,28,29,30,32	NC	No Connection
37	CTRL1	Can be configured as power-down input pin(active high),or as OVR output pin for channel A, depending on the register bit PDN/OVR FOR CTRL PINS.With an internal 50-kΩ pull-down resistor
12	CTRL2	Can be configured as power-down input pin(active high),or as OVR output pin for channel B, depending on the register bit PDN/OVR FOR CTRL PINS.With an internal 50-kΩ pull-down resistor
22	RESET	Hardware reset.Active high,With an internal 50-kΩ pull-down resistor
18	SCLK	Serial interface clock input,With an internal 50-kΩ pull-down resistor
19	SDATA	Serial interface data input,With an internal 50-kΩ pull-down resistor
21	SDOUT	Serial interface data output,With an internal 20-kΩ pull-down resistor
20	SEN	Serial interface enable,With an internal 50-kΩ pull-down resistor.(for ADS42LB69, it has a pull-up resistor for this pin)
56,57	CLKOUTP CLKOUTM	Diffreential LVDS output clock
39-48,50-55	DA[14:0]P, DA[14:0]M	DDR LVDS output interface for Channel A
1-10,58-63	DB[14:0]P, DB[14:0]M	DDR LVDS output interface for Channel B
13,16,23,26,31,33,36,38	AVDD	Analog 1.8-V power supply
11,49,64	DRVDD	Digital 1.8-V power supply
Ground pad	GND	Ground

Note[1]: The digital ports RESET,SCLK,SDATA,SDOUT,SEN,CTRL1,CTRL2,only can support 1.8V logic level

TIMING SPECIFICATIONS

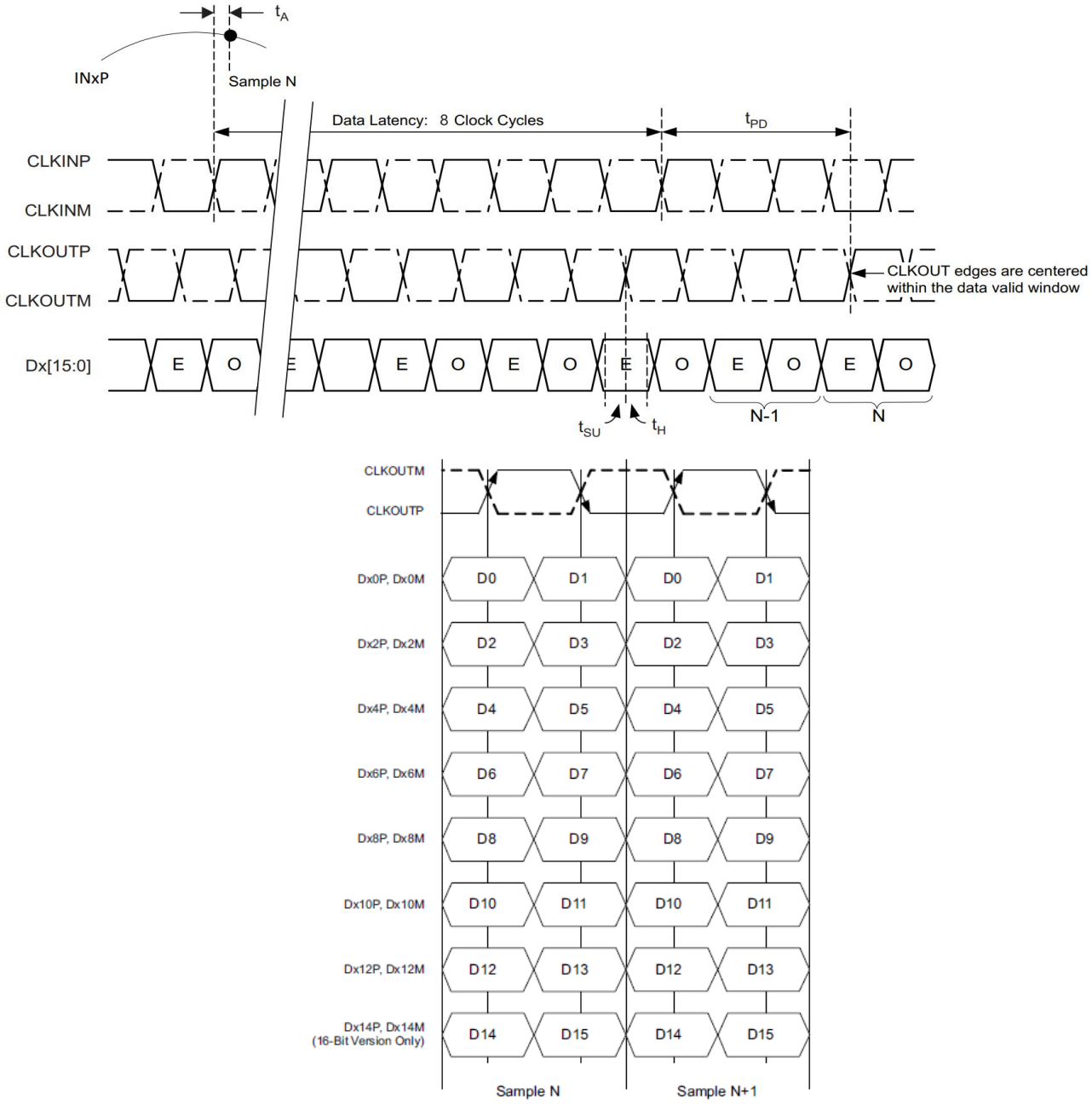

Figure 3 .DDR LVDS Output Timing Diagram

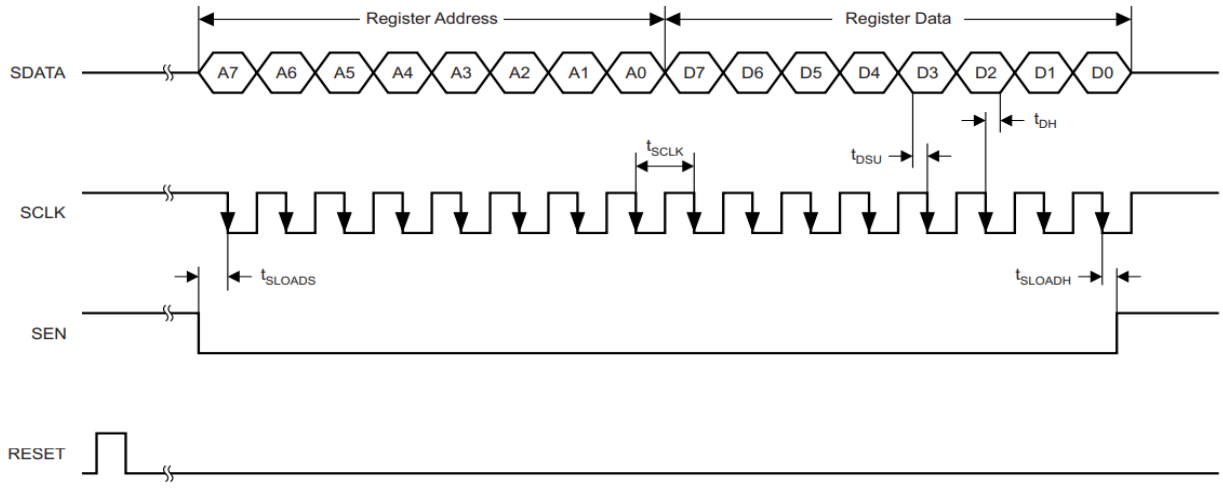

Figure 4 .Serial Register Wirting Timing Diagram

Serial Register Readout

The device includs a mode where the contents of the internal registers can be read back.The readback mode can be useful as a dignostic check to verify the serial interface communication between the external controller and ADC.

1. Set the READOUT register bit to1.This setting disable any further writes to the registers expect register address 00h
2.Iniate a serial interface cycle specifying the address of the register(A[7:0]whose content must be read
3.The device outputs the contents (D[7:0])of the selected register on the SDOUT terminal
4.The external controller can latch the contents at the SCLK falling edge
5.To enable register writes,reset the READOUT register bit to 0

Figure 4 illustrates these steps.When READOUT is diasabled,the SDOUT pin is in a high-impedance mode.If serial readout is not used,the SDOUT pin must float.

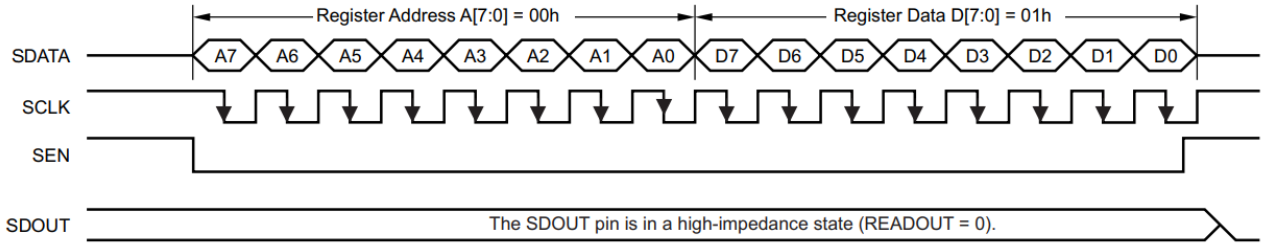

Figure 5 (1) .Enable Serial Readout(READOUT=1)

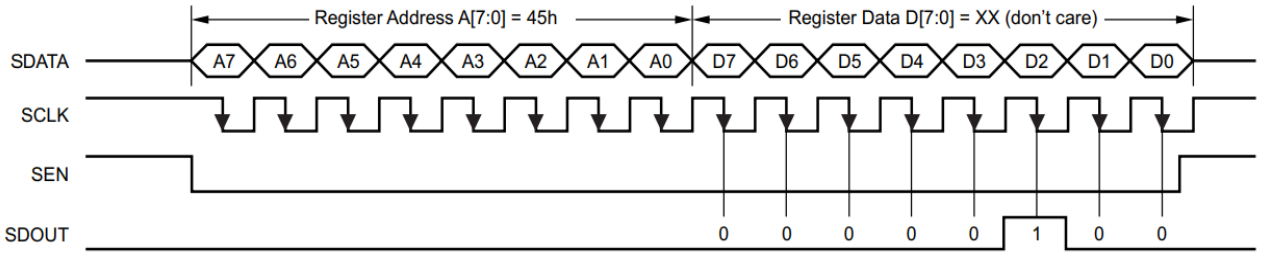

Figure 5 (2) .Read contents of Register 45h.The register is initialized with 04h.

Figure 5 . Serial Readout Timing Diagram

Register Maps

Table7. Register Table

REGISTER ADDRESS	Register Data							
ADDR(Hex)	D7	D6	D5	D4	D3	D2	D1	D0
03	0	TSTP_EN	TSTP_MODE	PDN_OVR	0	0	0	0
07	0	0	0	0	0	DITHER_ER	0	0
08	0	BK_CAL	0	0	0	FORE_CAL	1	1
16	FORMAT	0	LVDS_LV<5>	LVDS_LV<4>	LVDS_LV<3>	LVDS_LV<2>	LVDS_LV<1>	LVDS_LV<0>
17	0	0	0	1	DCO_DLY<1>	DCO_DLY<0>	0	0

Table8. Register 03 Field Description

Bit	Field	Defaults	Description
D[7]	-	0	Write'0'
D[6]	TSTP_EN	0	Output test pattern enable,active high.
D[5]	TSTP_MODE	0	Output test pattern mode selection: ‘ 0’ : Outputs toggle pattern: Data are an alternating sequence of 1001100110011001 and 0110011001100110. ‘ 1’ : Outputs toggle pattern: Data are an alternating sequence of 1010101010101010 and 0101010101010101.
D[4]	PDN_OVR	0	Determine CTRL1,CTRL2 as power-down control pin(input pin)，or OVR(output pin)： ‘ 0 ’ : CTRL1 and CTRL2 function as input pins, act as power-down control, active high ‘ 1 ’ : CTRL1 and CTRL2 function as output pins, act as overrange indications for AB channel. When the analog input over ranged, OVR pin output 1, otherwise OVR pin output 0.
D[3:0]	-	0000	Write'0'

Table9. Register 07 Field Description

Bit	Field	Defaults	Description
D[7:3]	-	0000	Write'0'
D[2]	DITHER_EN	0	'1': dithering on '0': dithering off
D[1:0]	-	00	Write'0'

Table10. Register 08 Field Description

Bit	Field	Defaults	Description
D[7]	-	0	Write'0'
D[6]	BK_CAL	0	'1': background calibration on '0': background calibration off
D[5:3]	-	000	Write'0'

D[2]	FORE_CAL	0	Active rising edge '1': foreground calibration on '0': foreground calibration off
D[1:0]	-	11	Write '1'

Table11. Register 16 Field Description

Bit	Field	Defaults	Description
D[7]	FORMAT	0	Output data format selection '0':offset binary output mode '1':twos complement output mode
D[6]	-	0	Write'0'
D[5:0]	LVDS_LV<5:0>	011001	'001011': LVDS output swing 160mV '011001': LVDS output swing 350mV (default) '011110': LVDS output swing 420mV '100001': LVDS output swing 470mV '100111': LVDS output swing 560mV

Table12. Register 17 Field Description

Bit	Field	Defaults	Description
D[7:5]	-	000	Write'0'
D[4]	-	1	Write'1'
D[3:2]	DCO_DLY<1:0>	01	'00': default-500ps '01': default '10': default +250ps '11': default +500ps
D[1:0]	-	00	Write'0'

Table13. Recommended settings for user

Foreground Calibration

ADDR(Hex)	Value
0×11	0×01
0×16	0×04
0×08	0×03
0×08	0×07
0×13	0×5b

Dither on

ADDR(Hex)	Value
0×07	0×04

Note . Dither should be opened 1ms after the frontground configuration is completed

EQUIVALENT CIRCUITS

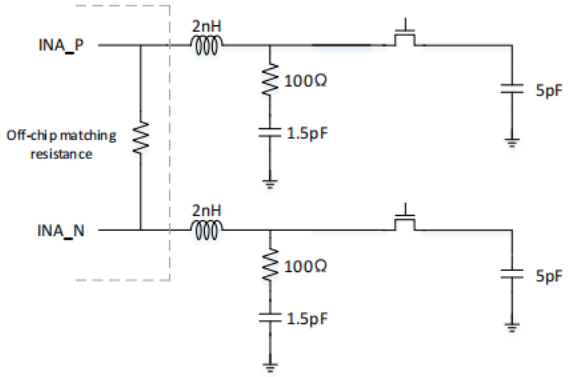

Figure 6. Equivalent Analog Input Circuit
(On the right side of the dashed line is in-chip)

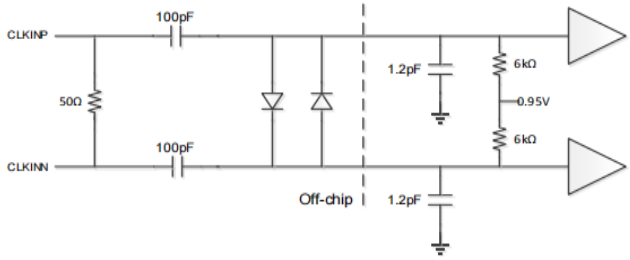

Figure 7. Equivalent Clock Input Circuit
(On the right side of the dashed line is in-chip)

Using a 4:1 impedance ratio transformer to increase the driving swing is beneficial for reducing clock jitter. The common mode bias of the clock input is provided internally.

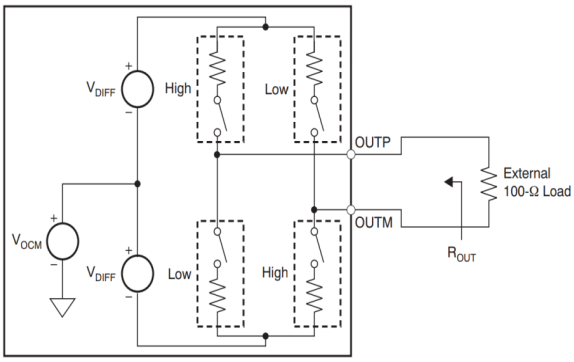

Figure 8. Equivalent LVDS Output Circuit

DRIVING CIRCUIT

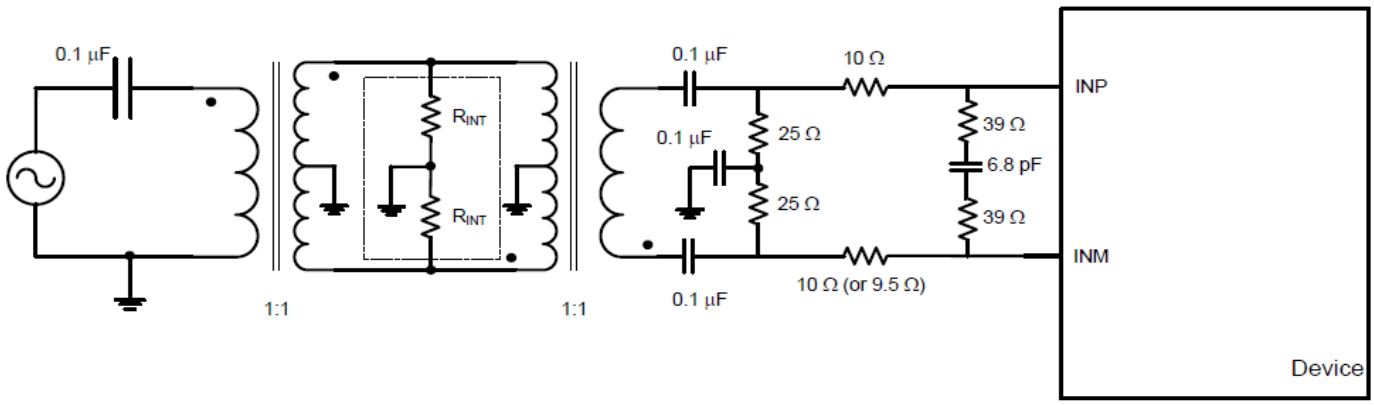

Figure 9.Drive circuit for analog input terminal
When the input frequency < 250M

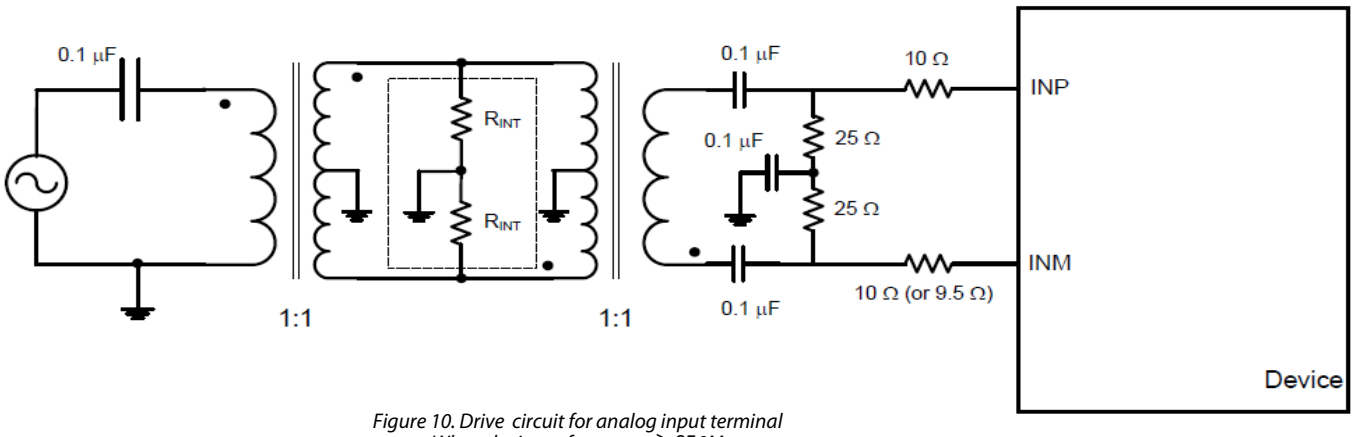

Figure 10. Drive circuit for analog input terminal
When the input frequency ＞250M

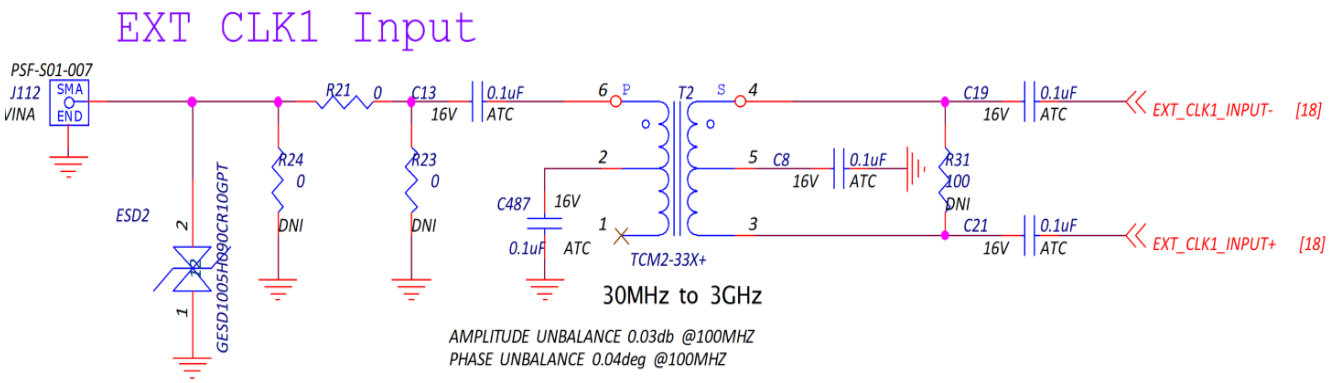

Figure 11. D r i v e Circuit for Clock Input

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the MCA42LB69 as asyste-m , it is recommended that the designer become familiar with t-hese guidelines, which describes the special circuit connections and layout requirements that are needed for certain pins.

POWER AND GROUND RECOMMENDATIONS

When connecting power to the MCA42LB69, it is ereconnded that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the MCA42LB69-250.With proper decoupling and smart partitioni-ng the PCB analog, digital, and clock sections, optimum performance is easily achieved.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the MCA42LB69. An exposed continuous copper plane on the PCB should mate to the MCA42LB69 exposed pad, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, whereas using one continuous plane with no partitions only guarantees one tie point. See Figure 1 2 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at www.analog.com.

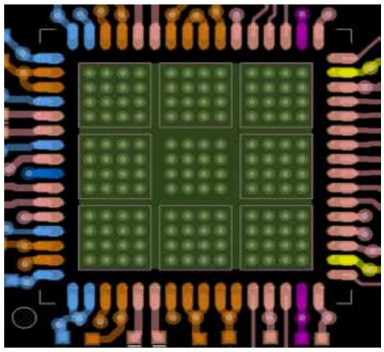

Figure 12.Typical PCB Layout

LVDS OUTPUT LINE PCB DESIGN RECOMMENDATIONS

When designing the PCB,be sure to equalize the equal length of the LVDS output of the output lines(both within and between differential pairs)can result in the formation of serious timing errors when the ADC is sampled by a data-receiving device,such as an FPGA.The output digital signals and accompanying clocks are output as LVDS differential pairs,and the differential outputs conform to the ANSI-644 LVDS standard.The LVDS driver current is derived from the chip,and the output current is set to a nomial 3.5mA at each output.The LVDS receiver inputs have a 100Ω differential termination resistor so that the receiver swing has a nominal value of the 350mV(or 700 mV p-p differential) the ADC LVDS output facilitates easy interface with custom ASICs and LVDS receiver interface in FPGAs for excellent switching performace in high noise environments.It is recommend to use a signal point-to-point network topology and place the 100Ω termination resistor as close to the receiver as possible.Timing errors may result if there is no remote receive termination resistor,or if the differential alignment is poorly routed.To avoid timing errors,it is recommended that alignment lengths not exceed 24 inches and that differential output alignments be as close to each other as possible and of equal length.

OUTLINE DIMENSIONS

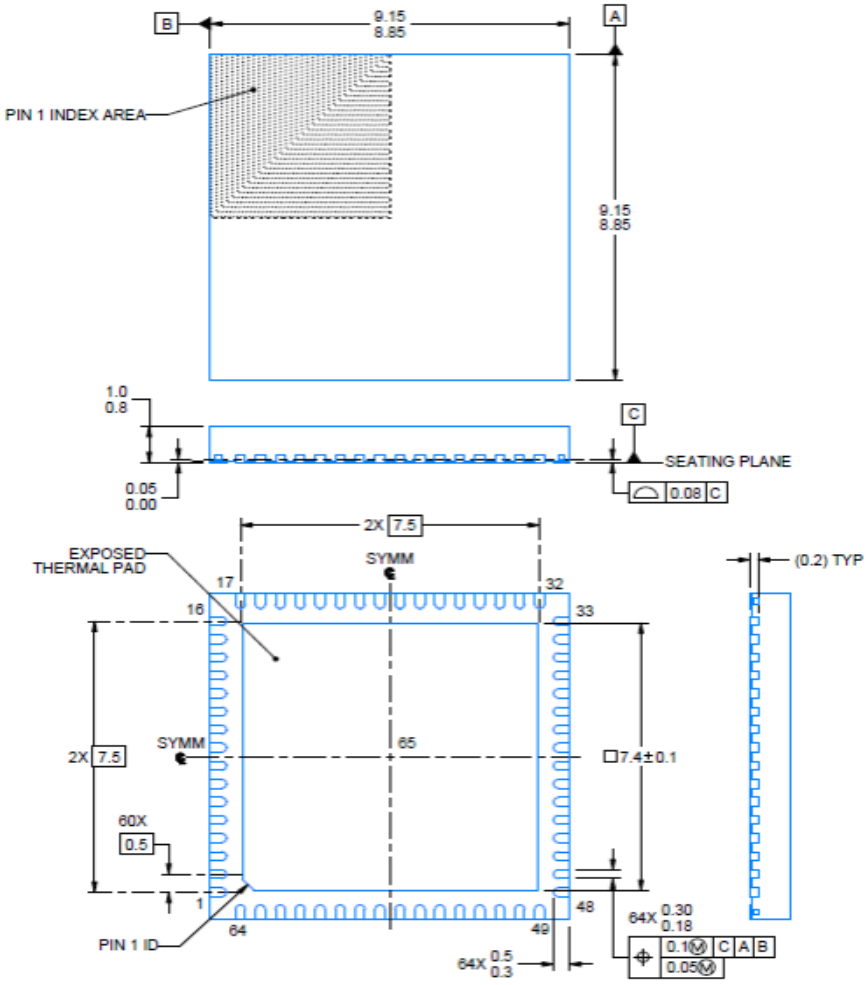

*Figure 13.VQFN-64 (9*9mm)*
All linear dimensions are in millimeters

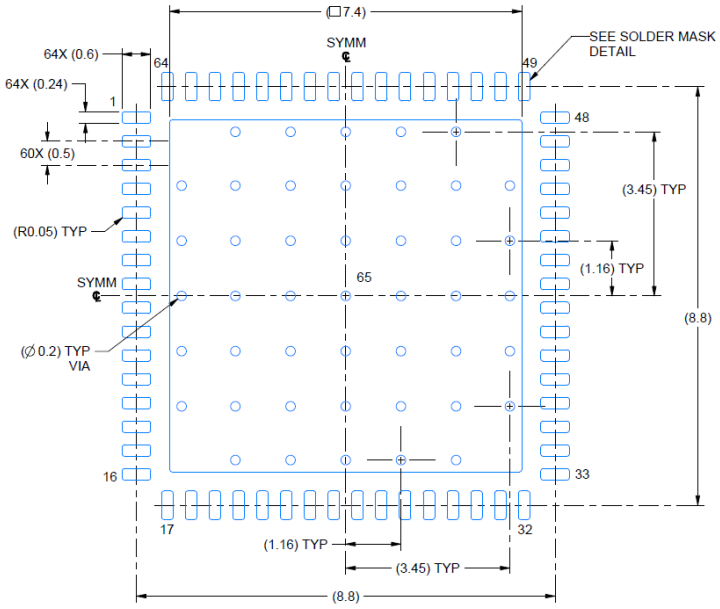

Figure 14.LAND PATTERN EXAMPLE

TYPICAL PERFORMANCE

Test conditions: TA=25 ℃, AVDD=1.8V，DRVDD=1.8V， Clock duty cycle is 50%, Sampling rate is 250MSPS.

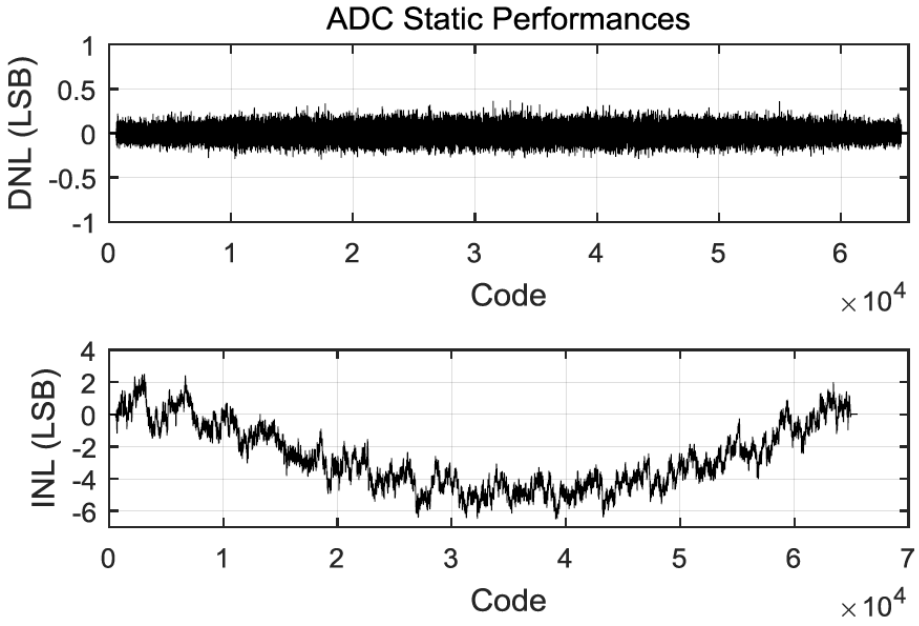

Figure 15.Typical static preformance(fin=70MHz,@250Ms/s)

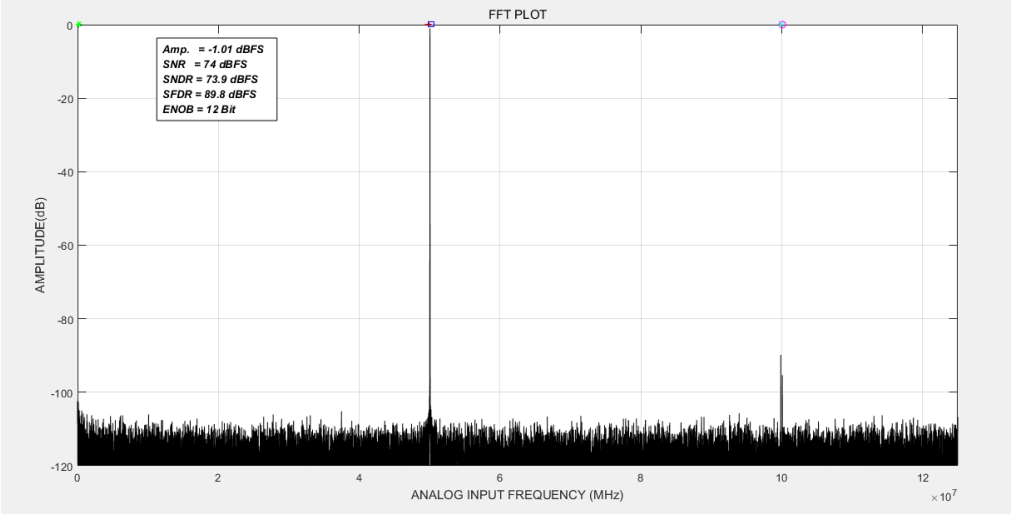

*Figure 16.A*_CHANNEL FIN=50M AMP=-1dBFs

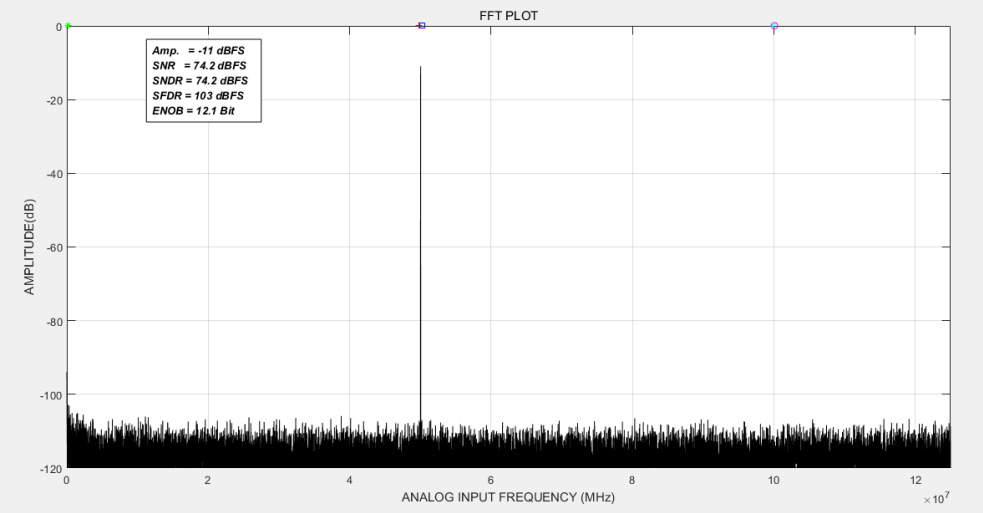

*Figure 17.A*_CHANNEL FIN=50M AMP=-11dBFs

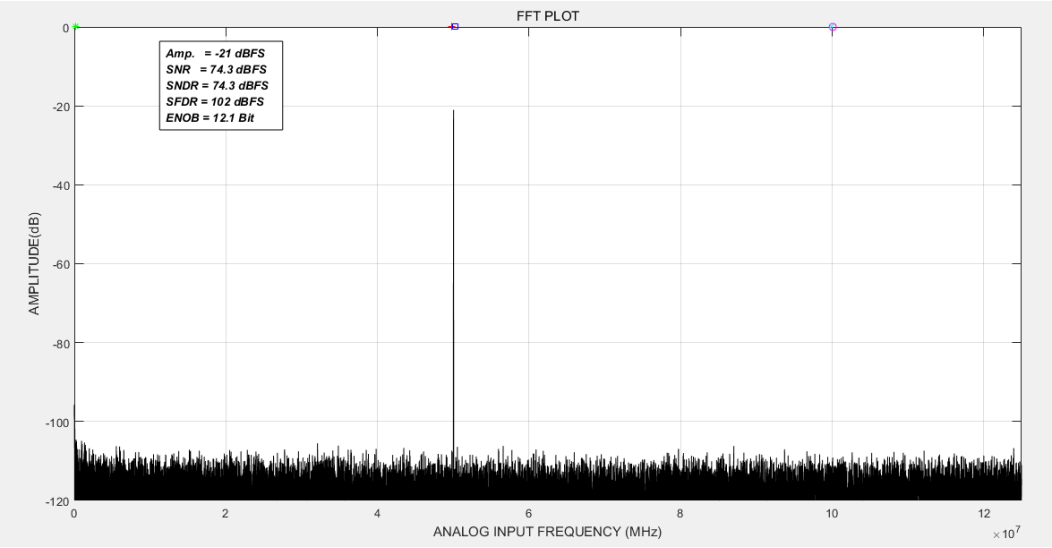

*Figure 18.A*_CHANNEL FIN=50M AMP=-21dBFs

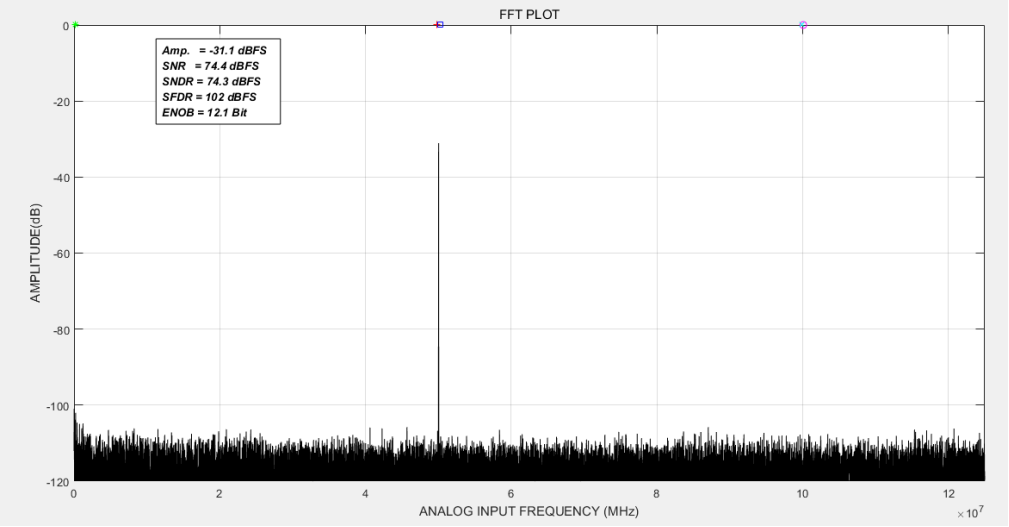

*Figure 19.A*_CHANNEL FIN=50M AMP=-31dBFs

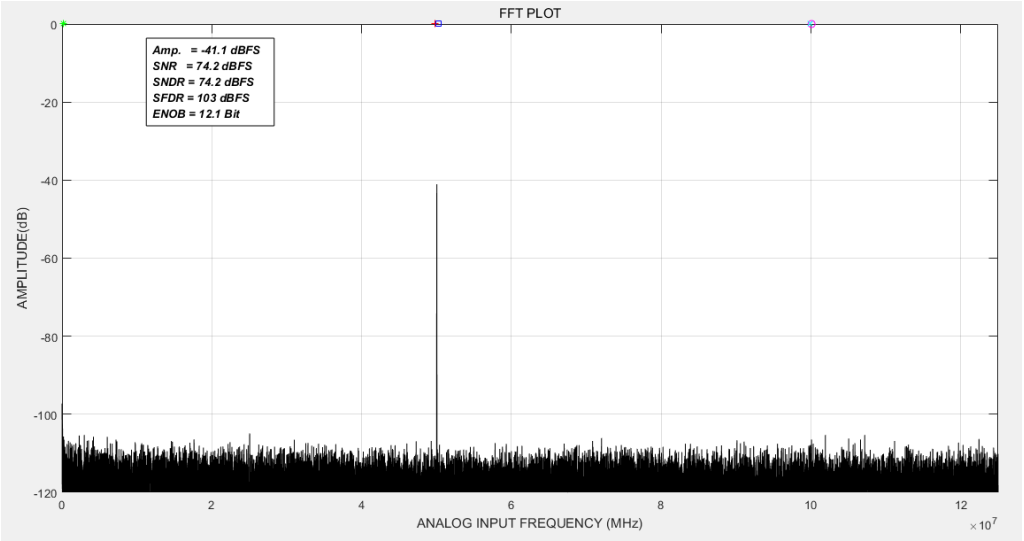

*Figure 20.A*_CHANNEL FIN=50M AMP=-41dBFs

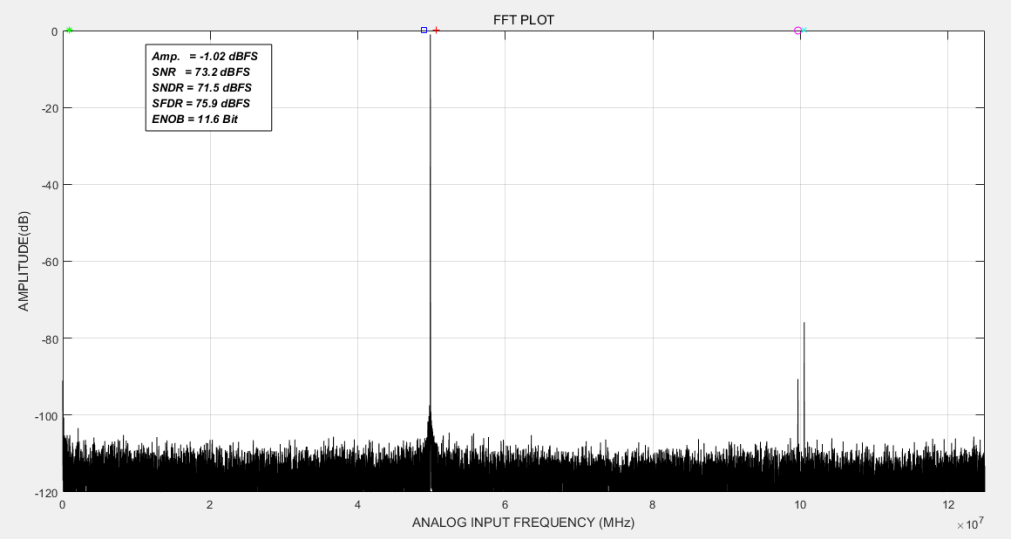

*Figure 21.B*_CHANNEL FIN=200M AMP=-21dBFs

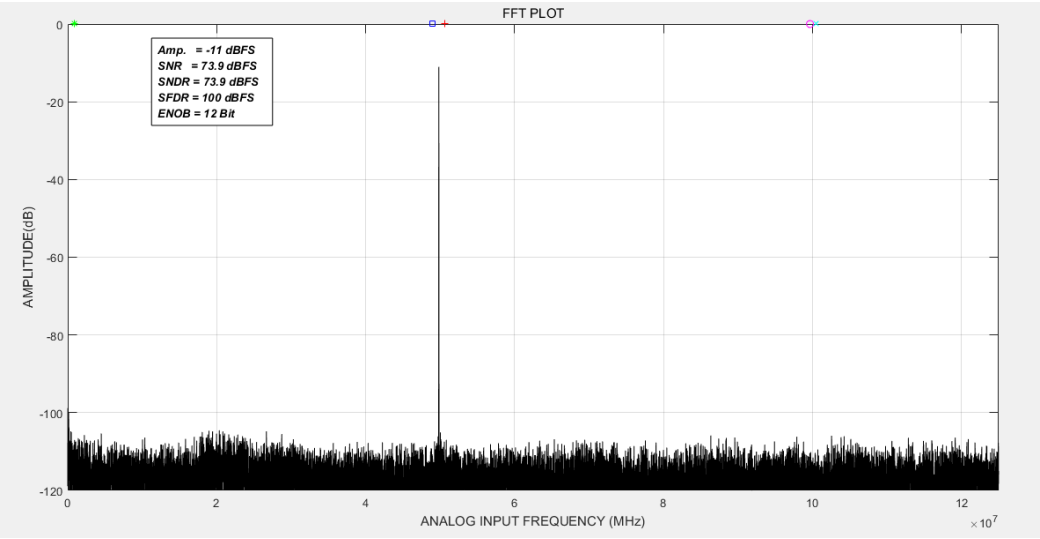

*Figure 22.B*_CHANNEL FIN=200M AMP=-31dBFs

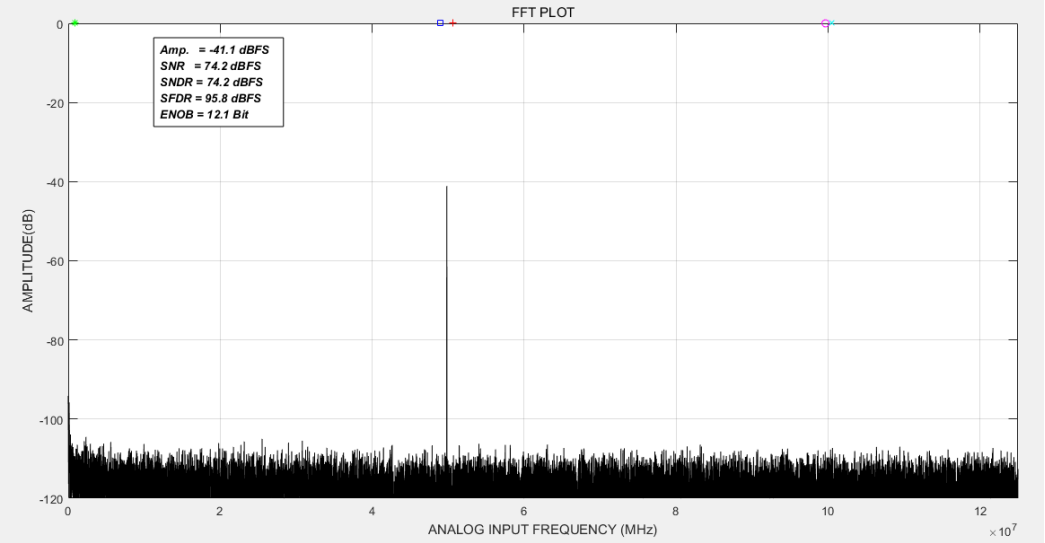

*Figure 23.B*_CHANNEL FIN=200M AMP=-41dBFs