Quad, 14-Bit, 125MSPS, Serial LVDS 1.8V Analog-to-Digital Converter

Data Sheet **MCA9253-125**

FEATURES

1.8 V supply operation
Low power: 120 mW per channel at 125 MSPS
SNR = 74.5dBFs(70MHz,2.0Vp-p input span)
SNR=75.5dBFs(70MHz,2.6Vp-p input span)
SFDR = 90 dBFs(to Nyquist,2.0V p-p input span)
DNL = ±0.7 LSB; INL = ±2 LSB (2.0 V p-p input span)
Serial LVDS and Low power,reduced signal option
650 MHz full power analog bandwidth
2V p-p input voltage range(Supports up to 2.6V)
Serial port control
Pin-compatible with AD9253-125

APPLICATIONS

Medical ultrasound
High speed imaging
Quadrature and diversity radio receivers
Test equipment

FUNCTIONAL BLOCK DIAGRAM

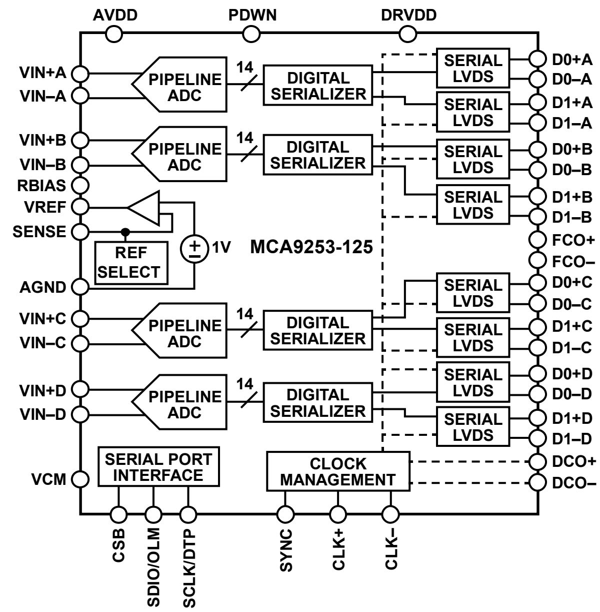

Figure 1.

GENERAL DESCRIPTION

The MCA9253-125 is a quad,14-bit, 125 MSPS analog-to-digital converter (ADC) with an on-chip sample-and-hold circuit designed for low-cost,low power,small size,and ease of use.The procuct operates at a conversion rate of up to 125MSPS and is optimized for outstanding dynamic performance and low power in applications where a small package size is cirtical.

The ADC requires a signle 1.8V power supply and LVPECL/ CMOS/LVDS compatible sample rate clock for full performance operation.No external reference or driver components are required for many applications.

The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate.A data clock output(DCO) for capturing data on the output and a frame clock output(FCO)for signaling a new output byte are provided.Individual-channel power-down is supported and typically consumes less than 2mW when all channels are disabled.The ADC contains several features designed to maximize flexibility and minimize system cost,such as programmable output clock and data alignment and digital test pattern generation.

The avaliable digital test patterns include built-in deterministic and pseudorandom patterns,along with custom user-defined test patterns entered via the serial port interface(SPI).

The MCA9253-125 is available in a RoHS-compliant.48-lead VQFN.It is specified over the industrial temperature range of -40°C to +85°C.

PRODUCT HIGHLIGHTS

1. Small Footprint.Four ADCs are contained in a small,space -saving package.
2. Low Power --Consumes only 120mW @125MSPS.
3. Ease of use --A data clock output(DCO) operates at frequencies of up to 500MHz and supports double data rate(DDR) operation.
4. User Flexibility--The SPI control offers a wide range of flexible features to meet specific system requirements.
5. Pin-Compatible --Pin-Compatible with AD9653(16 bits) AD9253(14 bits) and AD9633(12bits).

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V,2V p-p differential input,1.0V internal reference ,DCS close,unless otherwise noted.

Table 1.

Parameter	Temp	Min	Typ	Max	Unit
RESOLUTION			14		Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	-0.49	-0.3	0.17	%FSR
Offset Matching	Full	-0.14	+0.2	0.39	%FSR
Gain Error	Full	-8	-5	2.37	%FSR
Gain Matching	Full	1.0	1.1	1.5	%FSR
Differential Nonlinearity(DNL)	Full	-0.77		0.95	LSB
	25°C		±0.7		LSB
Integral Nonlinearity (INL)	Full	-4		4	LSB
	25°C		±3.5		LSB
TEMPERATURE DRIFT					
Offset Error	Full		3.5		ppm/°C
INTERNAL VOLTAGE REFERENCE					
Output Voltage(1V Mode)	Full	0.98	1.0	1.01	V
Load Regulation at 1.0mA (VREF=1.0V)	Full		2		mV
Input Resistance	Full		7.5		kΩ
INPUT-REFERRED NOISE					
VREF=1.0V	25°C		2.7		LSB rms
ANALOG INPUTS					
Differential Input Voltage (VREF=1.0V)	Full		2		Vp-p
Common-Mode Voltage	Full		0.9		V
Differential Input Resistance	25°C		2.6		kΩ
Differential Input Capacitance	25°C		7		pF
POWER SUPPLY					
AVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
IAVDD[1]	Full		305	330	mA
IDRVDD(ANSI-644 Mode)	Full		60	64	mA
IDRVDD(Reduced Range Mode)	25°C				
TOTAL POWER CONSUMPTION					
DC Input	Full		607	649	mW
Sine Wave Input(Four Channels including Output Drives ANSI-644 Mode)	Full		657	780	mW
Sine Wave Input(Four Channels including Output Drives Reduced Range Mode	25°C		630		mW

DC SPECIFICATIONS

Table 1 Continued.

Power-Down	Full		2		mW
Standby[3]	Full		356	392	mW

[1.]Measured with a low input frequency,full scale sine wave on all four channels.

[2.]Can be controlled via the SPI .

AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V,2V p-p differential input,1.0V internal reference ,DCS close,unless otherwise noted.

Table 2 .

Parameter	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO(SNR)					
fIN=9.7MHz	25°C		76		dBFs
fIN=15MHz	25°C		75.8		dBFs
fIN=70MHz	Full	73.5	74.5		dBFs
fIN=128MHz	25°C		71.9		dBFs
fIN=200MHz	25°C		70.5		dBFs
SIGNAL-TO-NOISE-AND-DISTORTION RATIO(SINAD)					
fIN=9.7MHz	25°C		78		dBFs
fIN=15MHz	25°C		77.7		dBFs
fIN=70MHz	Full	74.6	76.1		dBFs
fIN=128MHz	25°C		73.6		dBFs
fIN=200MHz	25°C		70.3		dBFs
EFFECTIVE NUMBER OF BITS(ENOB)					
fIN=9.7MHz	25°C		12.7		Bits
fIN=15MHz	25°C		12.6		Bits
fIN=70MHz	Full	12.1	12.4		Bits
fIN=128MHz	25°C		11.9		Bits
fIN=200MHz	25°C		11.4		Bits
SPURIOUS-FREF DYNAMIC RANGE(SFDR)					
fIN=9.7MHz	25°C		96		dBc
fIN=15MHz	25°C		93		dBc
fIN=70MHz	Full	78	89		dBc
fIN=128MHz	25°C		87		dBc
fIN=200MHz	25°C		77		dBc
WORST HARMONIC(SECOND OR THIRD)					
fIN=9.7MHz	25°C		-98		dBc
fIN=15MHz	25°C		-93		dBc
fIN=70MHz	Full	-78	-89		dBc
fIN=128MHz	25°C		-87		dBc
fIN=200MHz	25°C		-77		dBc

DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V,2V p-p differential input,1.0V internal reference ,DCS close,unless otherwise noted.

Table 2. Continued.

WORST OTHER(EXCULDING SECOND OR THIRD)					
fIN=9.7MHz	25°C		-96		dBc
fIN=15MHz	25°C		-98		dBc
fIN=70MHz	Full	-85	-94		dBc
fIN=128MHz	25°C		-89		dBc
fIN=200MHz	25°C		-83		dBc
TWO-TONE INTERMODULATION DISTORION(IMD)-AIN1 AND AIN2=-7.0dBFs					
fIN1=70.5MHz,fIN2=72.5MHz	25°C		-90		dBc
CROSSTALK[1]	25°C		91		dB
CROSSTALK(OVERRANGE CONDITION)[2]	25°C		87		dB
POWER SUPPLY REJECTION(PSRR)[3]					
AVDD	25°C		31		dB
DRVDD	25°C		79		dB
ANALOG INPUT BANDWIDTH (FULL POWER)	25°C		650		MHz

[1].Crosstalk is measured at 70MHz with -1.0dBFs analog input on one channel and no input on the adjacent channel.
[2].Overrange condition is specified as being 3dB above the full-scale input range
[3].PSRR is measured by injecting a sinusoidal signal at 10MHz to the power supply pin and measuring the output supr on the FFT.PSRR is calculated as the ratio of the amplitudes of the spur voltage over the pin voltage,exprssed in decibels.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V,unless otherwise noted.

Table 3 .

Parameter	Temp	Min	Typ	Max	Unit
CLOCK INPUTS(CLK+,CLK-)					
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage[1]	Full	0.2		3.6	Vp-p
Input Voltage Range	Full	AGND-0.2		AGND+0.2	V
Input Common-ModeVoltage	Full		0.9		V
Input Resistance(Differential)	25°C		15		V
Input Capacitance	25°C		4		pF
Logic INPUT(PDWN,SYNC,SCLK)					
Logic 1 Voltage	Full	1.2		AVDD+0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		30		kΩ
Input Capacitance	25°C		2		pF
Logic INPUT(CSB)					
Logic 1 Voltage	Full	1.2		AVDD+0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		2		pF

Table 3 . Continued.

Logic INPUT(SDIO)[2]					
Logic 1 Voltage	Full	1.2		AVDD+0.2	V
Logic 0 Voltage	Full	0		0.8	V
Input Resistance	25°C		26		kΩ
Input Capacitance	25°C		5		pF
Logic OUTPUT(SDIO)					
Logic 1 Voltage(I_{OH}=800uA)	Full		1.79		V
Logic 0 Voltage(I_{OL}=50uA)	Full			0.05	V
DIGITAL OUTPUTS(D0±x,D1±x),ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage(V_{OD})	Full	290	345	400	mV
Output Offset Voltage(V_{OS})	Full	1.15	1.25	1.35	V
Output Coding(Default)			Twos complement		
DIGITAL OUTPUTS (D0±x,D1±x),LOW POWER,REDUCED SIGNAL OPTION					
Logic Compliance			LVDS		
Differential Output Voltage(V_{OD})	Full	160	200	230	mW
Output Offset Voltage(V_{OS})	Full	1.15	1.25	1.35	mW
Output Coding(Default)			Two complement		V

1. This is specified for LVDS and LVPECL only.
2. This is specified for 13 SDIO/OLM pins sharing the same connection.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V,unless otherwise noted.

Table 4 .

Parameter	Temp	Min	Typ	Max	Unit
CLOCK					
Input Clock Rate	Full	20		1000	MHz
Conversion Rate	Full	20		125	MSPS
Clock Pulse Width High(t_{EH})	Full		4.00		ns
Clock Pulse Width Low (t_{EL})	Full		4.00		ns
Output PARAMETERS[1]					
Propagation Delay(t_{PD})	Full		2.3		ns
Rise Time(t_R)(20% to 80%)	Full		300		ps
Fall Time(t_F)(20% to 80%)	Full		300		ps
FCO Propagation Delay(t_{FCO})	Full	1.5	2.3	3.1	ns
DCO Propagation Delay(t_{CPD})[2]	Full		t_{FCO} +(t_{SAMPLE}/14)		ns
DCO to Data Delay (t_{DATA})[2]	Full	(t_{SAMPLE}/14) - 300	(t_{SAMPLE}/14)	(t_{SAMPLE}/14) + 300	ps
DCO to FCO Delay(t_{FRAME})[2]	Full	(t_{SAMPLE}/14) - 300	(t_{SAMPLE}/14)	(t_{SAMPLE}/14) + 300	ps
Lane Delay(t_{LD})			90		ps
Data to Data Skew(t_{DATA_MAX}-t_{DATA_MIN})	Full		±50	±200	ps
Wake-up Time(Standby)	25°C		250		ns

Table 4 . Continued.

Wake-up Time(Power-Down)[3]	25°C		375		us
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay(t_A)	25°C		1		ns
Aperture Uncertainty(Jitter,t_j)	25°C		135		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

1.Can be adjusted via the SPI.The conversion rate is the clock rate after the divider.

2.t_{SAMPLE}/14 is based on the number of bits in two LVDS data lanes.t_{SAMPLE}= 1 / f s

3.Wake-up time is defined as the time required to return to normal operation from power-down mode.

Table 5 .

Parameter	Description	Limit	Unit
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.24	ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.40	ns typ
SPI TIMING REQUIR			
t_{DS}	Setup time between the data and the rising edge of SCLK	2	ns min
t_{DH}	Hold time between the data and the rising the edge of SCLK	2	ns min
t_{CLK}	Period of the SCLK	40	ns min
t_S	Setup time between CSB and SCLK	2	ns min
t_H	Hold time between CSB and SCLK	2	ns min
t_{HIGH}	SCLK pulse width high	10	ns min
t_{LOW}	SCLKpulse width low	10	ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10	ns min
t_{DIS_SDIO}	Time require for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10	ns min

Timing Diagrams

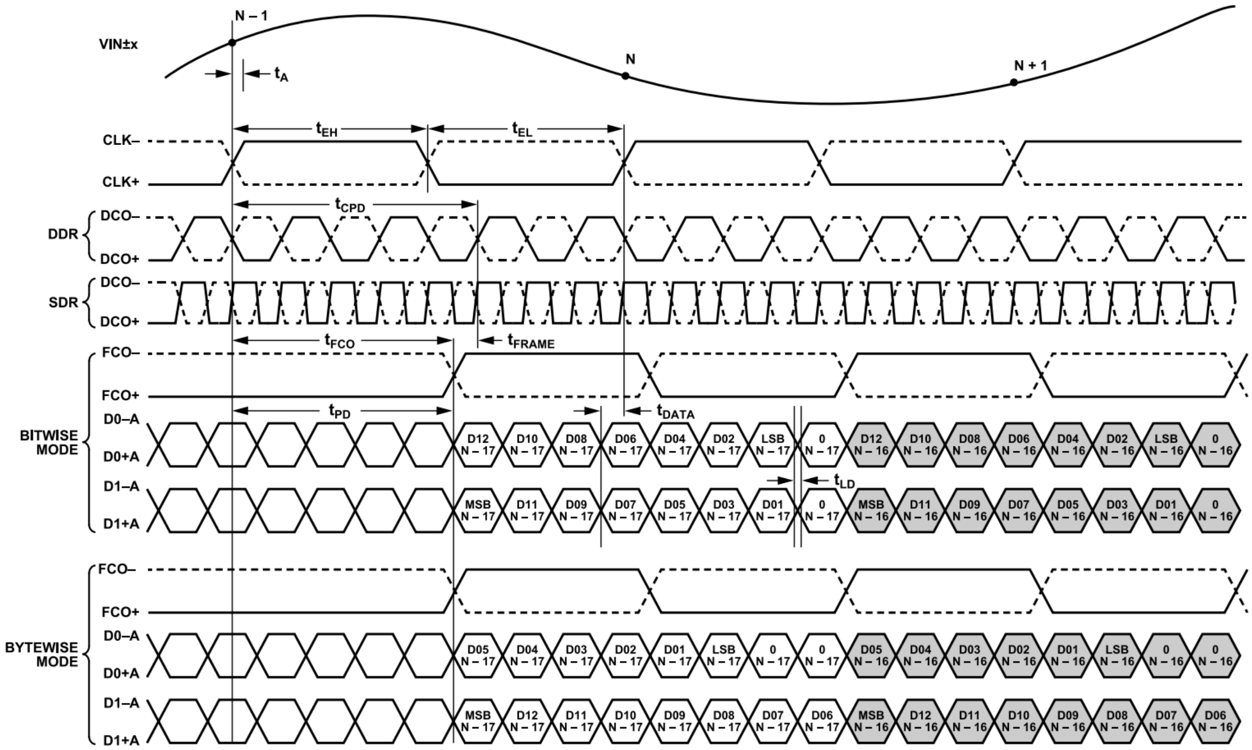

Figure 2.16-Bit DDR/SDR,Two-Lane,1×Frame Mode(Default)

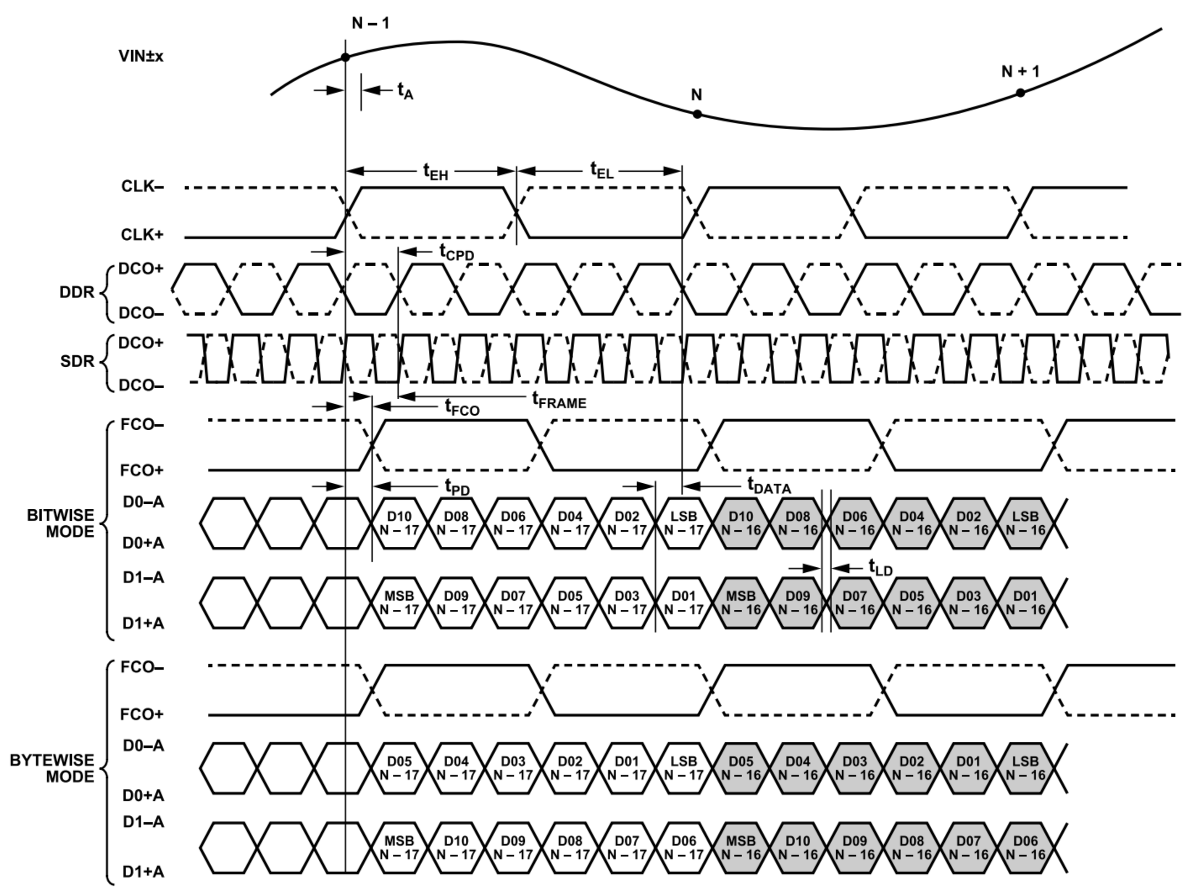

Figure 3.12-Bit DDR/SDR,Two-Lane,1×Frame Mode

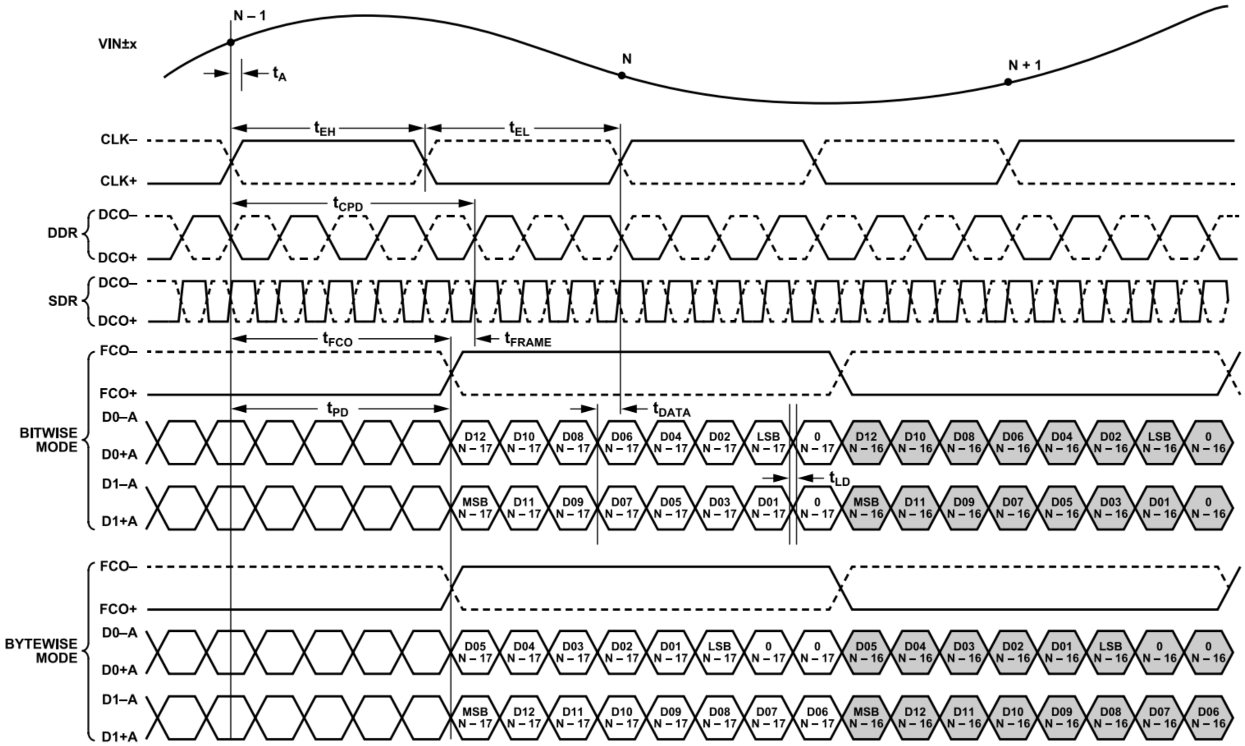

Figure 4.16-Bit DDR/SDR,Two-Lane,2×Frame Mode

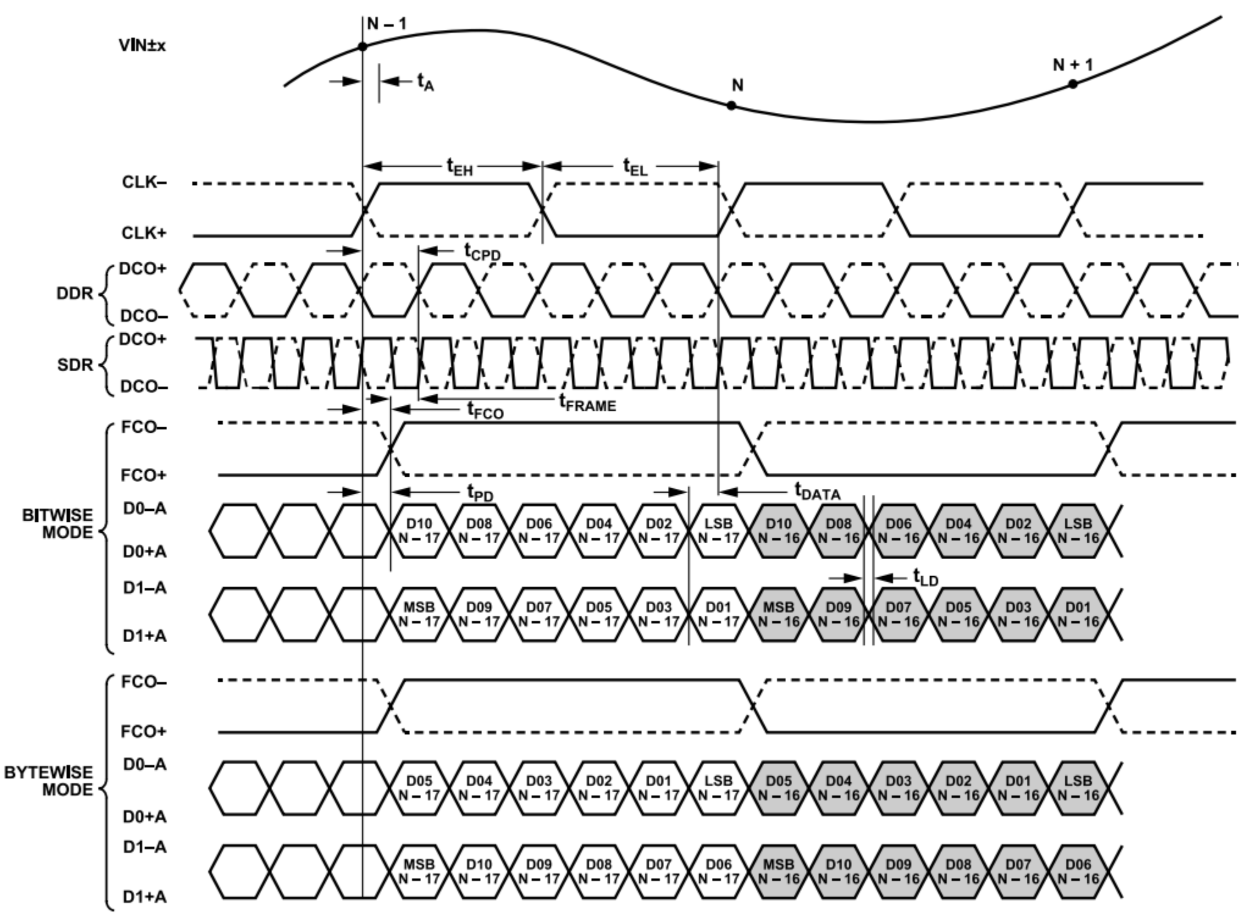

Figure 5.12-Bit DDR/SDR,Two-Lane,2×Frame Mode

Timing Diagrams

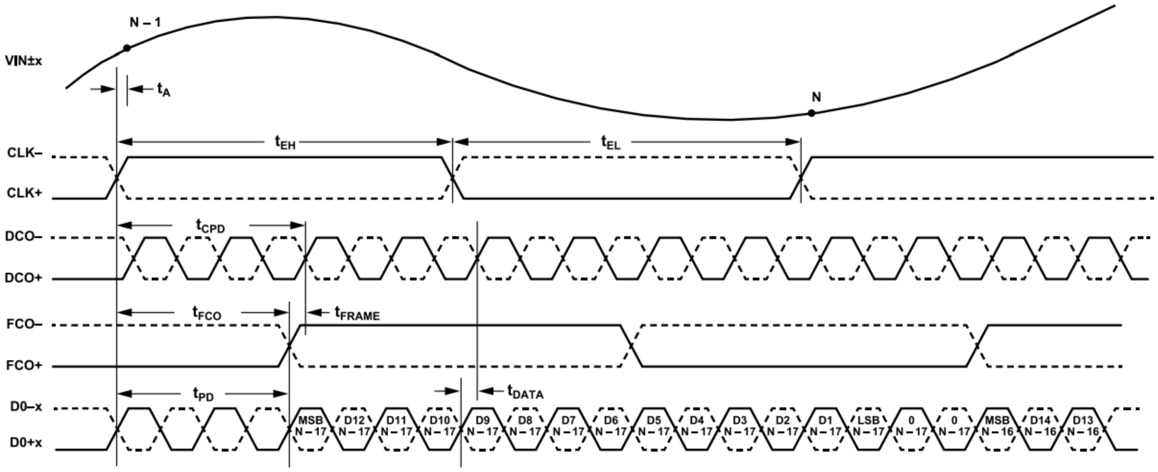

Figure 6.Wordwise DDR/SDR,Two-Lane,2×Frame Mode

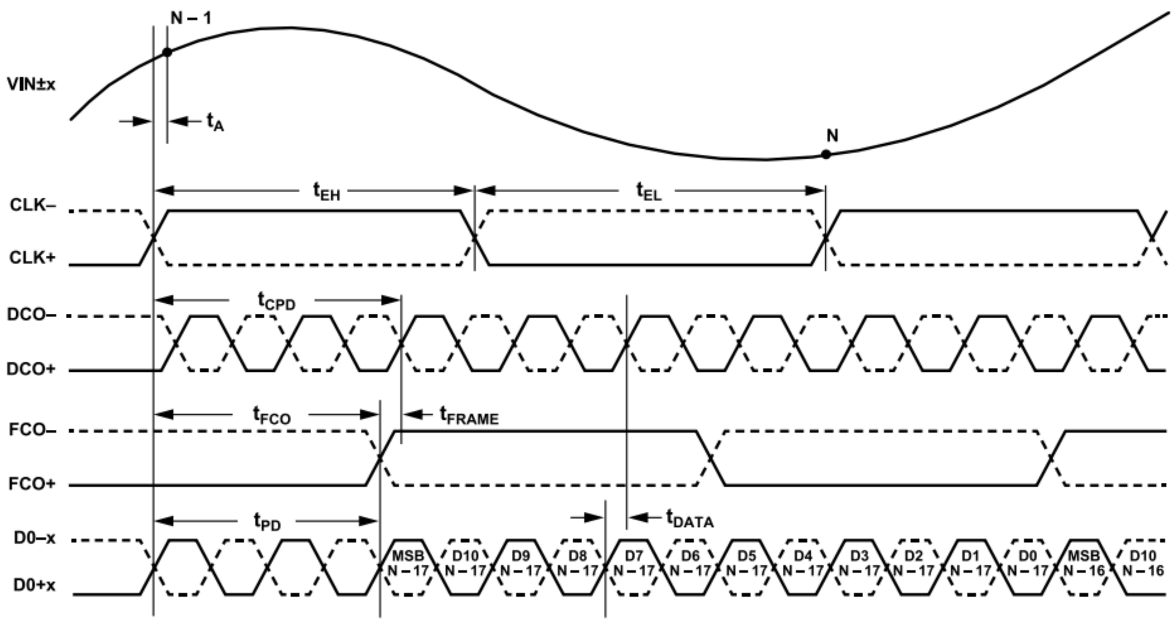

Figure 7.Wordwise DDR ,One-Lane,1×Frame,12-Bit Output Mode

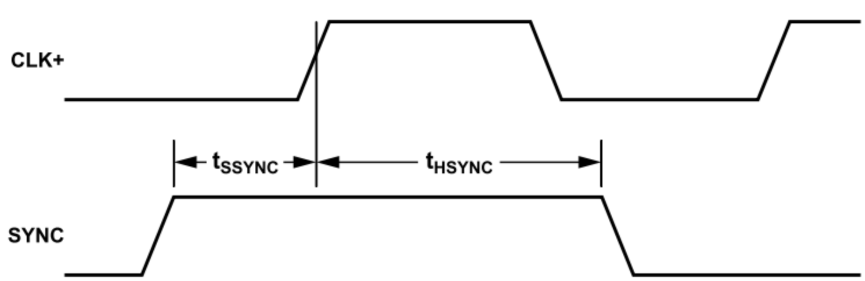

Figure 8.SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
Digital Outputs (D0±x, D1±x, DCO+, DCO−, FCO+, FCO−) to AGND	−0.3 V to +2.0 V
Analog Iutputs	
CLK+, CLK− to AGND	−0.3 V to +2.0 V
VIN+x, VIN−x to AGND	−0.3 V to +2.0 V
SCLK/DTP, SDIO/OLM, CSB to AGND	−0.3 V to +2.0 V
SYNC, PDWN to AGND	−0.3 V to +2.0 V
RBIAS to AGND	−0.3 V to +2.0 V
VREF, SENSE to AGND	−0.3 V to +2.0 V
Environmental	
Operating Temperature Range	-55°C to 150°C
Maximum Junction Temperature	150°C
Lead Temperature	300°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 7.ESD Level

		Max	Unit
$V_{(ESD)}$Electrostatic discharge	HBM,MIL-STD-883K/ Method3015.9	±2500	V
$V_{(ESD)}$Electrostatic discharge	CDM,ESDA/JEDEC JS-002-2018	±1000	V

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

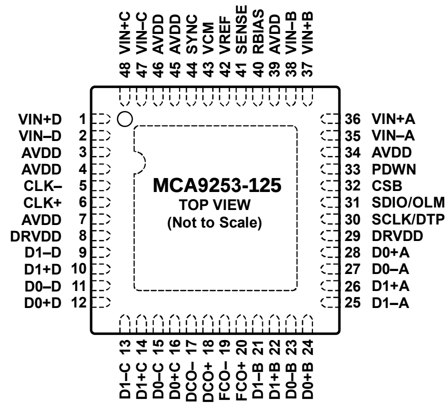

Figure 9 . 48-Lead VQFN Pin Configuration, Top View

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
0	AGND, Exposed Pad	Analog Ground, Exposed Pad. The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
1	VIN+D	ADC D Differential Input True.
2	VIN−D	ADC D Differential Input Complement.
3, 4, 7, 34, 39, 45, 46	AVDD	1.8 V Analog Supply Pins.
5, 6	CLK−, CLK+	Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.
8, 29	DRVDD	Digital Output Driver Supply.
9, 10	D1−D, D1+D	Channel D Digital Outputs.
11, 12	D0−D, D0+D	Channel D Digital Outputs.
13, 14	D1−C, D1+C	Channel C Digital Outputs.
15, 16	D0−C, D0+C	Channel C Digital Outputs.
17, 18	DCO−, DCO+	Data Clock Outputs.
19, 20	FCO−, FCO+	Frame Clock Outputs.
21, 22	D1−B, D1+B	Channel B Digital Outputs.
23, 24	D0−B, D0+B	Channel B Digital Outputs.
25, 26	D1−A, D1+A	Channel A Digital Outputs.
27, 28	D0−A, D0+A	Channel A Digital Outputs.
30	SCLK/DTP	SPI Clock Input/Digital Test Pattern.
31	SDIO/OLM	SPI Data Input and Output Bidirectional SPI Data/Output Lane Mode.
32	CSB	SPI Chip Select Bar. Active low enable; 30 kΩ internal pull-up.
33	PDWN	Digital Input, 30 kΩ Internal Pull-Down. PDWN high = power-down device. PDWN low = run device, normal operation.
35	VIN−A	ADC A Differential Input Complement.
36	VIN+A	ADC A Differential Input True.
37	VIN+B	ADC B Differential Input True.
38	VIN−B	ADC B Differential Input Complement.
40	RBIAS	Sets Analog Current Bias. Connect to 10 kΩ (1% tolerance) resistor to ground.
41	SENSE	Reference Mode Selection.
42	VREF	Voltage Reference Input and Output.
43	VCM	Analog Output at Midsupply Voltage. Sets the common mode of the analog inputs, external to the ADC,
44	SYNC	Digital Input. SYNC input to clock divider.
47	VIN−C	ADC C Analog Input Complement.
48	VIN+C	ADC C Analog Input True.

THEORY OF OPERATION

The MCA9253-125 is a multistage ,pipelined ADC.Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The serializer transmits this converted data in a 14-bit output. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples.Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The data is then serialized and aligned to the frame and data clock.

ANALOG INPUT CONSIDERATIONS

The analog input to the MCA9253-125 is a differential switched-capaci -tor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellt performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

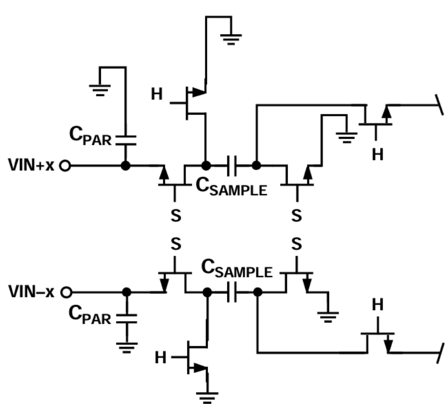

Figure 10.Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample mode and hold mode (see Figure 10). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle,A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and therefore achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front

The clock signal alternately switches the input circuit between front end at high IF frequencies. Either a differential capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise

INPUT COMMON MODE

The analog inputs of the MCA9253 are not internally dc-biased ,Therefore ,in ac-coupled applictions,the user must provide this bias externally.Setting the device so that V_{CM} =AVDD/2 is recommended for optimum performance,but the device can function over a wider range with reasonable performance.

An on-chip,common-mode voltage reference is included in the design and is available form the V_{CM} pin .The VCM pin must be decoupled to ground by a 0.1uF capacitoe,as described in the Applications Information section.

Maxium SNR performance is achieved by setting the ADC to the largest span in a diferential configuation.

DIFFERENTIAL INPUT CONFIGURATIONS

There are several ways to drive the MCA9253-125 either actively or passively.However,optimum performance is achieved by driving the analog inputs differentially.Using a differential double balun configuration to drive the MCA9253-125 provides excellent perforamce and a flexible interface to the ADC for baseband applications(see Figure11).For applications where SNR is a key parameter,differential transformer coupling is the recommended input configuration (see Figure 12),because the noise performance of most amplifiers is not adequate to achieve the true performance of the MCA9253-125.Regardless of the configuration,the value of the shunt capacitor C,is dependent on the input frequency and may need to be reduced or removed.It is not recommended to drive the MCA9253-125 inputs single-ended.

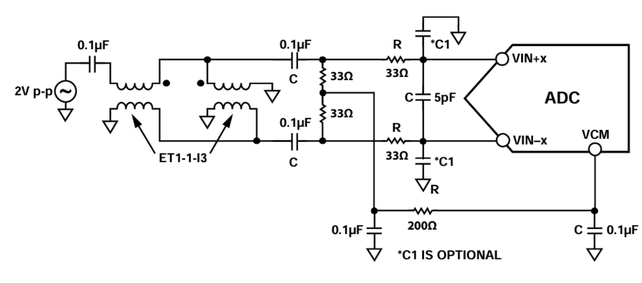

Figure 11.Differential Double Balun Input Configuration for Baseband Applications

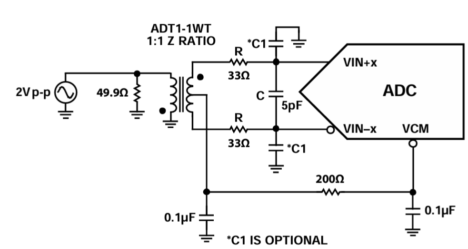

Figure 12.Differential Transformer-Coupled Configuration for Baseband Applications

VOLTAGE REFERENCE

A stable and accurate 1.0V voltage reference is built into the MCA -9253 .VREF can be configured using either the internal 1.0V reference or an externally applied 1.0V reference voltage.The various reference modes are summarized in the Internal Reference Connection section and the External Reference Operation section.The VREF pin must be externally decoupled to ground with a low ESR,1.0uF capacitor in parallel with a low ESR, 0.1uF ceramic capacitor.

INTERNAL REFERENCE CONNECTION

A comparator within the MCA9253 detects the potential at the SENSE pin and configures the reference into three possible modes .which are summarized in Table 9 .If SENSE is grounded,the reference amplifier switch is connected to the internal resistor divider(see Figure 13),setting VREF to 1.0V.If SENSE is connected to an external resitive voltage divider (see Figure 14),then VREF is defined as follows:

VREF =0.5×(1+R2/R1)

which

7kΩ≤(R1+R2)≤10kΩ

Table 9 .Reference Configuraton Summary

Selected Mode	SENSE Voltage (V)	Resulting VREF (V)	Resulting Differential Span(Vp-p)
Fixed Internal Reference	AGND to 0.2	1.0 internal	2.0
Programmable Internal Reference	Connect external R-divider(see figure14)	0.5×(1+R2/R1), such as:R1=3. 5kΩ,R2=5.6kΩ (VREF=1.3V)	2×VREF
Fixed External Reference	AVDD	1.0 to 1.3V, applied to external VREF pin	2.0 to 2.6

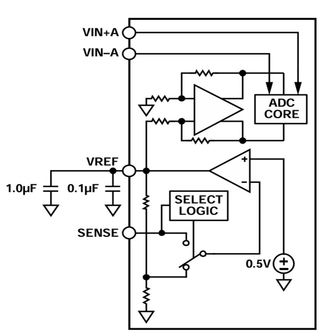

Figure 13.
1.0V Internal Reference Configuration

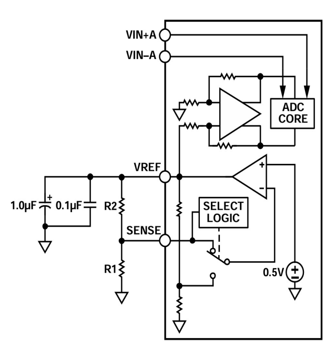

Figure 14.
Programmable Internal Reference Congiuration

EXTERNAL REFERENCE

The use of an extenal reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics.When the SENSE pin istied to AVDD,the internal reference is disabled,allowing the use of an external reference.An internal reference buffer loads the external reference with an equivalent 7. 5KΩ load.The internal buffer generates the positive and negative full-scale references for theADC core .It is not recommended to leave the SENSE pin floating.

CLOCK INPUT CONSIDERATIONS

For optimum performance,clock the MCA9253-125sample clock inputs,CLK+ and CLK- pins via a transformer or capacitors.These pins are biased internally and require no external bias.

Clock Input Options

The MCA9253-125 has a flexible clock input structure.The clock input can be a CMOS,LVDS, LVPECL,or sine wave signal.Regardless of the type of signal being used,clock source jitter is of the most concern,as described in the Jitter Consideration section.

Figure 15 and 16 show two preferred methods for clocking the MCA9253-125(at clock rates up to 1GHz prior to internal CLK divider).A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

The RF balun configuration is recommended for clock frequencies between 125MHz and 1GHz,and the RF transformer is recommended for clock frequencies from 20MHz to 200MHz.The anti-parallel Schottky diodes across the transformer/ balun secondary winding limit clock excursions into the MCA9253-125 to approximately 0.8-Vp-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the MCA9253-125 while preserving the fast rise and fall times of the signal that are critical to achieving low jitter performance.However,the diode capacitance comes into play at frequencies above 500MHz.Care must be taken in choosing the appropriate signal limiting diode.

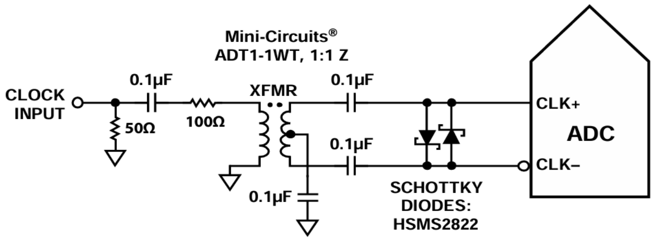

Figure 15.Transformer-Coupled Differential Clock (Up to 200MHz)

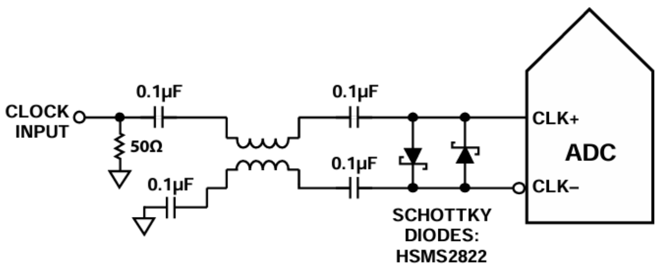

Figure 16.Balun-Coupled Differential Clock (Up to 1GHz)

If a low jitter clock source is not available,another option is to ac couple a differential PECL signal to the sample clock input pins,as shown in Figure 17.

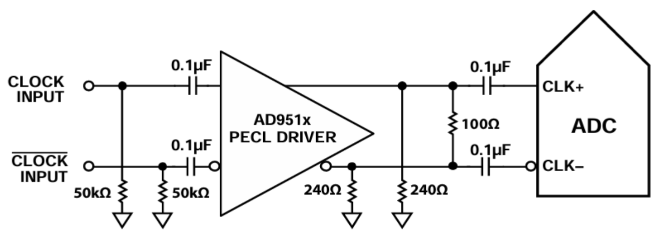

Figure 17.Differenital PECL Sample Clock (Up to 1GHz)

A third option is to ac couple a differential LVDS signal to the samp -le clock input pins,as shown in Figure 18.

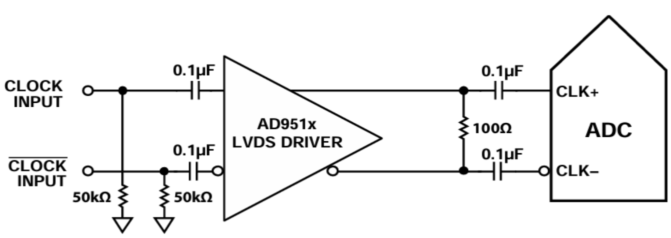

Figure 18.Differenital LVDS Sample Clock (Up to 1GHz)

In some applications,it may be acceptable to drive the sample clock inputs with a signle-ended 1.8V CMOS signal.In such applications, drive the CLK+ pin directly from a CMOS gate,and bypass the CLK - pin to ground with a 0.1uF capacitor(see Figure 19).

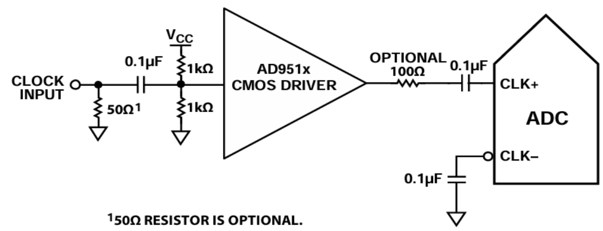

Figure 19.Single-Ended 1.8V CMOS Input Clock (Up to 200MHz)

Input Clock Divider

The MCA9253-125 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8.

The MCA9253-125 clock divider can be synchronized using the external SYNC input.Bit0 and Bit1 of Register 0×109 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written.A valid SYNC causes the clock divider to reset to its iniaial state.This synchronization feature allows multiple parts to hav their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and,as a result,may be sensitive to clock duty cycle.Commonly,a ±5% tolaerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The MCA9253 contains a duty cycle stabilizer(DCS)that retimes the nonsampling(falling)edge,providing an internal clock signal with a nominal 50% duty cycle.This allos the user to provide a wide range of clock input duty cycles without affecting the performance of the MCA9253 -125.Noise and disortion performance are nearly flat for a wide range of duty cycles with the DCS on.Jitter in the rising edge of the input is still of concern and is not easily reduced by the internal stabilization circuit.The duty cycle control loop does not function for clock rates less than 20MHz,nominally.The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically.A wait time of1.5us to 5us is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal.

Jitter Considerations

High speed ,high resolution ADCs are sensitive to the quality of the clock input.The degradation in SNR at a given input frequency(fA) due only to aperture jitter(tJ) can be calculated by:

SNR Degradation=a

In this equation,the rms aqerture jitter represents the root sum square of all jitter sources,including the clock input,analog input signal,and ADC aperture jitter specifications.IF undersampling applications are particularly sensitive to jitter.

The clock input must be treated as an analog signal in cases where aperture jitter can be affect the dynamic range of the MCA9253. Power supplies for clock drives must be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise,Low jitter ,crystal-controlled oscillators make the best clock sources.If the clock is generated from another type of source(by gating dividing,or other methods),it must be retimed by the original clock at the last step.

POWER DISSIATION AND POWER-DOWN MODE

The power dissipated by the MCA9253-125 is proporional to its sample rate.The digital power dissipation does not vary significantly because it is determined primarity by the DRVDD supply and bias current of the LVDS output drivers.

The MCA9253-125 is placed in power-down mode either by the SPI port or by asserting the PDWN pin high.In this state,the ADC typically dissipates 2mW.During power-down ,the output drivers are placed in a high impedance state.Asserting the PDWN pin low retures the MCA9253-125 to its normal opperating mode .Note that PDWN is referenced to the analog supply(AVDD)and must not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference,reference buffer,biasing networks, and clock,Internal capacitors are discharges when entering power -down node and then must be recharged when returning to normal operation.As a result,wake-up time is related to the time spent in power-down mode,and shorter power-down cycles result in proportionally shorter wake-up times.When using the SPI port interface,the user can place the ADC in power-down node or standby mode.Standby mode allows the user to keepthe internal reference circuit powered when faster wake-up times are required .See the Memory Map section for more details on using these features.

DIGITAL OUTPUTS AND TIMING

The MCA9253-125 differential outputs conform to the ANSI-644 LVDS standard on default power-up.This can be changed to a low power,reduced signal option(similar to the IEEE 1596.3 standard)via the SPI.The LVDS driver current is derived on chip and sets the output current at each output equal to a nominal 3.5mA.A 100Ω differential termination resistor placed at the LVDS receiver intputs results in a nominal 350mV(or 700mV p-p differential)at the receiver.

When operating in reduced range mode,the output current is reduced to 2mA.This results in a 200mV swing (or 400mV p-p differential)across a100Ω termination at the receiver.

The MCA9253-125 LVDS outputs facilitate interfacing with LVDS receivers in custom ASICs and FPGAs for superior switching performance in noisy environments,Single point-to-point net tepoloies are recommended withe a 100Ω termi nation resistor placed as close to the receiver as possible.If there is no far-end receiver termination or there is poor differential trace routing,timing errors may result.To avoid such timing errors,it is recommended that the trace length be less than 24inchs and that the differential output traces be close together and at equal lengths.This can be achieved by programming Register 0×15.Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors,the power dissipation of the DRVDD supply increases when this option is used.

The format of the output data is twos complement by default.An example of the output coding format can be found in Table 1 0 .To change the output data format to offset binary,see the Memory Map section.

Data from each ADC is serialized and provided on a separate channel in DDR mode.The data rate of each serial stream is equal to 14bits times the sample clock rate divided by the number of lanes,with a miximum of 500Mbps/lane(14bits×125MSPS)/(2×2)=500MSPS/lane.

The lowest typical conversion rate is 20MSPS.Two output clocks are provided to assist in capturing data from the MCA9253-125.The DCO is used to clock the output data and is equal to four times the samples clock(CLK)rate for the default mode of operation.Data is clocked out of the MCA9253-125 and must be captured on the rising and falling edges of the DCO that supports double data rate (DDR)catpturing.The FCO is used to signal the start of new output byte and is equal to the sample clock rate in1×frame mode.See the Timing Diagrams section for more information.

Table 10 .Digital Output Coding

Input(V)	Condition(V)	Offset Binaty Output Mode	Twos Complement Mode
VIN+ -VIN-	＜-VREF - 0.5LSB	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ -VIN-	-VREF	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ -VIN-	0V	1000 0000 0000 0000	0000 0000 0000 0000
VIN+ -VIN-	+VREF-1.0LSB	1111 1111 1111 1100	0111 1111 1111 1100
VIN+ -VIN-	＞+VREF - 0.5LSB	1111 1111 1111 1100	0111 1111 1111 1100

Table 11.Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattren Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select	Notes
0000	off(default)	N/A	N/A	N/A	
0001	Midscale short	1000 0000 0000 0000(16-bit)	N/A	Yes	Offset binary code shown
0010	+Full-scale short	1000 0000 0000 0000(16-bit)	N/A	Yes	Offset binary code shown
0011	-Full -scale short	1010 1010 1010 1010(16-bit)	0101 0101 0101 0101(16-bit)	Yes	Offser binary code shown
0100	Checkerboard	1010 1010 1010 1010(16-bit)	0101 0101 0101 0101(16-bit)	No	
0101	PN sequence long	N/A	N/A	Yes	PN23 ITU 0.150 $X^{23}+X^{18}+1$
0110	PN sequence short	N/A	N/A	Yes	PN9 ITU 0.150 $X^{9}+X^{5}+1$
0111	1-/0-bit toggle	111 1111 1111 1100(16-bit)	0000 0000 0000 0000(16-bit)	No	
1000	User input	Register 0×19 to Register 0×1A	Register 0×1B to Register 0×1C	No	
1001	1-/0-bit toggle	1010 1010 1010 1000(16-bit)	N/A	No	
1010	1×sync	0000 0001 1111 1100(16-bit)	N/A	No	
1011	one bit high	1000 0000 0000 0000(16-bit)	N/A	No	Pattern associated with the external pin
1100	Mixed Frequency	1010 0001 1001 1100(16-bit)	N/A	No	

The PN short sequence test pattern generates a pseudorandom bit sequence that repeats every 2^{9}-1or 511 bits.The seed value is all 1s(the initial value is provided in Table 12).The output is a parallel representation of the PN9 sequence in MSB-first format.The first output word contains the first 14bits of the PN9 sequence in MSB-aligned form.

The PN long sequence test pattern generates a pseudorandom bit sequence that repeats every 2^{23}-1or 8,388,607 bits.The seed value is all 1s(the initial value is provided in Table 11).The output is a parallel representation of the PN23 sequence in MSB-first format.The first output word contains the first 14bits of the PN23 sequence in MSB-aligned form.

Table 12. PN Sequence

Sequence	Initial Value	This first three sampled outputs (MSB priority)binary complement
PN sequence short	0×1FE0	0×1DF1,0×3CCB,0×294E
PN sequence long	0×1FFF	0×1FE0,0×2001,0×1C00

SDIO/OLM PIN

For applications that do not require SPI mode operation,the CSB pin is tied to AVDD,and the SDIO/OLM pin controls the output lane mode according Table13.For applications where this pin is not used,CSB must be tied to AVDD.When using the one-lane mode,the encode rate must be ≤62.5MSPS to meet the maximum output rate of 1Gbps.

Table 13. Output Lane Mode Pin Settings

OLM Pin Voltage	Output Mode
AVDD(Default)	Two-lane,1×frame,16-bit serial output
GND	One-lane,1×frame,16-bit serial output

SCLK/DTP PIN

The SCLK/DTP pin is use for in applications that do not require SPI mode operation.This pin can enable a single digital test pattern if it and the CSB pin are held high during device power-up. When SCLK/DTP is tired to AVDD.the ADC channel outputs shift out the following pattern:1000 0000 0000 0000.The FCO and DCO function normally while all channels shift out the repeatable test pattern .This pattern allows the user to perform timing alignment adjustments among the FCO,DCO,and output data.This pin has an internal 10kΩ resistor to GND.It can be left unconnected.

Table 14.Digital Test Pattern Pin Settings

Selected DTP	DTP Voltage	Resulting D0±x and D1±x
Normal Operation DTP	10KΩ to AGND AVDD	Normal operation 1000 0000 0000 0000

CSB Pin

The CSB pin must be tied to AVDD for applictaions that not require SPI mode operation.By tying CSB high,all SCLK and SDIO information is ignored.Note that when the CSB pin is connected to AVDD, the device DCS is enabled by default and remains active until the device enters SPI mode and is configured via SPI. For further details regarding DCS, please refer to the Clock Duty Cycle section.

RBIAS Pin

To set the internal code bias current of the ADC,place a 10.0kΩ,1% tolerance resistor to ground at the RBIAS pin.

OUTPUT TEST MODES

The Output test options are described in Table 11 and controlled by the output test mode bits at Address 0×0D.When an output test mode is enabled,the analog section of the ADC is disconnected from the digital back-end blocks and the test patterns is run through the output formatting,and some are not.The PN generators from the PN sequence tests can be reset by setting Bit4 or Bit5 of Register signal (If present,the analog signal is ignored),But they do require an encode clock.

SERIAL PORT INTERFACE(SPI)

The MCA9253-125 serial port interface(SIP)allows the user to configuration the converter for specific functions or operations through a structured register space provided inside the ADC.The SPI offers the user added flexibility and customization,depending on the application.Addresses are accessed via the serial port and can be written to or read from via the port.Memory is organized into bytes that can be further divided into fileds,which are documented in the Memory Map section.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin,and the CSB pin,(see Table 15).The SCLK(a serial clock)is used to synchronized the read and write data presented form and to the ADC.The SDIO(serial data input/output)is a dual-purpose pin that allows data to sent to and read from the internal ADC memory map regiaters .The CSB (chip select bar)is an active low control that enables or disables the read and write cycles.

Table 15.Serial Port Interface Pins

Pin	Function
SCLK	Serial clock.The serial shift clock input,which is used to synchronize serial interface reads and writes.
SDIO	Serial data input/output.A dual-purpose pin typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip Select bar.An active low control that gates the read and write cycles.

The falling edge of the CSB,in conjunction with the rising edge of the SCLK,determines the start of the framing .An example of the serial timing and its definitions can be found in Figure 19 and Table 5.

Other modes involving the CSB are available.The CSB can be held low indefinitely,which permanently enables the device; this is called streaming.The CSB can stall high between bytes to allow for additional external timing.When CSB is tied high. SPI functions are placed in high impedance mode.This mode turns on any SPI pin secondary functions.

During an instruction phase,a 16-bit instruction is transmitted .Data follows the instruction phase,and its length is determined by the W0 and W1 bits

In additional to word length,the instruction phase determins whether the serial frame is a read or write operation,allowing the serial port to be used both to program the chip and to read the connents of the on-chip memory.The first bit of the first byte in a multibyte serial data transer frame indaicates whether a read command or a write command is issued.If the instruction is a readback operation,performing a readback causes the serial data input/output(SDIO)pin to change dircection from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words.Data can be sent in MSB-first mode or in LSB-first mode,MSB-first mode is the default on power -up and can be changed via the SPI port configuration register.

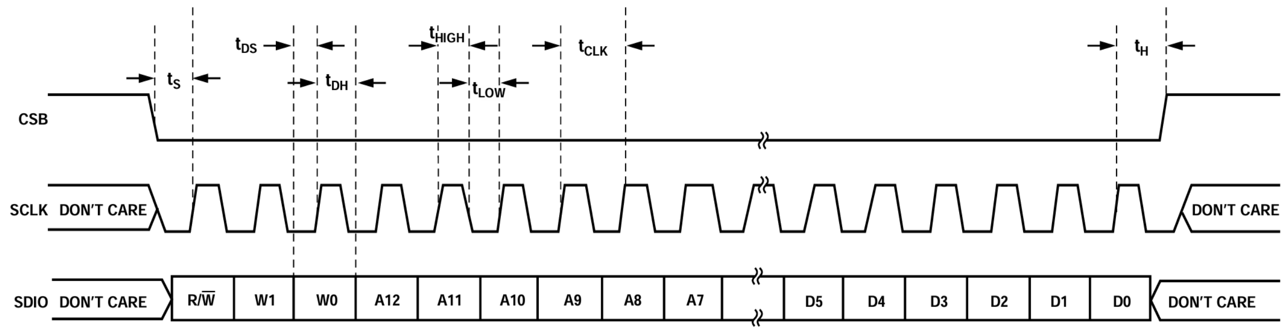

Figure 20.Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 14 comprise the physical interface between the user programming device and the serial port of the MCA9253-125.The SCLK pin and the CSB pin function as inputs when using the SPI interface.The SDIO pin is bidirectional,functioning as an input during write phases and as an output during readback.

The SPI interface is flexible is enough to be controlled by either FPGAs or microcontrollers .The SPI port must not be active during periods when the full dynamic performance of the converter is required.Because the SCLK signal,the CSB signal,and the SDIO signal are typically asynchronous to the ADC clock,noise from these signals can degrade converter performance .If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and MCA9253-125 to prevent these signals form transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI interface is not being used.When the pins are strapped to DRVDD or ground during device power-on,they are associated with a specific function.Table12 and 13 describes the strappable functions supported on the MCA9253-125.

CONFIGURATION WITHOUT THE SPI

In applications that do not require SPI control register inter -face,the SDIO/OLM pin ,the SCLK/DTP pin and PDWN pin function as independent CMOS-compatible control pins When the device is powered on ,if the user intends to use these pins as static control lines to mange the output channel mode,digital test code,and power-down features respectively, the CSB pin should be connected to AVDD in this mode to disable the serial port interface.

Note that when the CSB pin is connected to AVDD, the devices DCS is enabled by default and remains active until the device enters SPI mode and is configured via SPI. For more information on DCS, refer to the "Clock Duty Cycle section."

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI.

Table 16.Features Accessible Using the SPI

Feature Name	Description
Power Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS,set the clock divider,set the clock divider phase, and enable the sync
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test mode to have known data on ouputs bits
Output Mode	Allows the user to set the output mode
Output Phase	Allows the user to set the output polarity

MEMORY MAP

Table 17.Memory map rejister table

The MCA9253-125 uses a 3-wire interface and 16-bit addressing.Please refer to ADI Application Note: AN-877 interface with high Speed ADC via SPI.

ADDR (Hex)	Partmeter Name	Bits 7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)	Default Value (Hex)	Comments
Chip Configuration Registers											
0×00	SPI pin configuration	0=SDO active	LSB first	Soft reset	16-bit address	16-bit address	Soft reset	LSB first	0=SDO active	0×18	The nibbles are mirrored so that LSB-first or MSB-first mode registers correctly.The default for ADCs is 16-bit mode
0×01	Chip ID(global)	8-bit chip ID,Bits[7:0] MCA9253-125 0×8F=quad 14-bit 125MSPS serial LVDS								0×8F	Unique chip ID used to differentiate devices ;read only.
0×02	Open	Open	Open			Open	Open	Open	Open		Open
Device Index and Transfer Registers											
0×05	Device index	Open	Open	Clock Channel DCO	Clock Channel FCO	Data Channel D	Data Channel C	Data Channel B	Data Channel A	0×3F	Bits are set to determine which device on chip receives the next write command .The default is all devices on chip.
0×FF	Transfer	Open	Open	Open	Open	Open	Open	Open			
Global ADC Function Registers											
0×08	Power modes(global)	Open	Open	External power-down pin function 0= power-down 1=stand -by	Open	Open	Open	Power mode 00=chip run 01=full power-down 10=standby 11=reset		0×00	Determines various generic modes of chip operation.
0×09	Clock(global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilize 0=off 1=on	0×01	Turns duty cycle stabilizer on or off.
0×0B	Clock divide(global)	Open	Open	Open	Open	Open	Clock divide ratio[2:0] 000=divide by 1 001=divide by 2 010=divide by 3 011=divide by 4 100=divide by 5 101=divide by 6 110=divide by 7 111=divide by 8			0×00	

ADDR (Hex)	Parameter Name	Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)	Default Value (Hex)	Comments
0×0C	Open	Open	Open	Open	Open	Open	Chop Mode 0=off 1=on	Open	Open	0×00	Enable/disables chop mode
0×0D	Test mode(local expect for PN sequence resets)	User input test mode 00=signle 01=alternate 10=single once 11=alternate once (affects user input test mode only,Bits[3:0]=1000)		Rest PN long gen	Rest PN short gen	Output test mode[3:0](local) 0000=off(default) 0001=midscale short 0010=positive FS 0011=negative FS 0100=alternating checkboard 0101=PN 23 sequence 0110=PN 9 sequence 0111=one/zero word toggle 1000=user input 1001=1-/0- bit toggle 1010=1×sync 1011=one bit high 1100=mixed bit frequency				0×00	When set,the test data is placed on the output pins in place of normal data.
0×10	Offset adjust(local)	8-bit device offset adjustment[7:0](local) Offset adjust in LSBs from +127 to -128(twos complement format)								0×00	Device offset trim
0×14	Output mode	Open	LVDS-ANSI/ LVDS-IEEE option 0=LVDS-ANSI 1=LVDS-IEEE reduced range link (global)	Open	Open	Open	Output invert (local)	Open	Output format 0=offset binary 1=twos comple-ment (global)	0×01	Configures the outputs and the format of the data.
0×15	Output adjust	Open	Open	Output driver termination[1:0] 00=none 01=200 10=100 11=100		Open	Open	Open	Output drive 0= 1×drive 1= 2×drive	0×00	Determines LVDS or other output properties
0×16	Output phase	Open	Input clock phase adjust[6:4] (value is number of input clock cycles of phase delay);see table 8.			Output clock phase adjust[3:0](000 through 1011)				0×03	On devices that use global clock divide,determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.
0×18	VREF	Open	Open	Open	Open	Open	Internal VREF adjustment digital scheme[2:0] 000=1.0 V p-p 001=1.14 V p-p 010=1.33 V p-p 011=1.6 V p-p 100=2.0 V p-p			0×04	Selects and/or adjusts the VREF.

ADDR (Hex)	Parameter Name	Bit7 (MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (LSB)	Default Value (Hex)	Comments
0×19	USER_PATT1_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0×00	User Defined Pattern 1 LSB
0×1A	USER_PATT1_MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0×00	User Defined Pattern 1 MSB
0×1B	USER_PATT2_LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0×00	User Defined Pattern 2 LSB
0×1C	USER_PATT2_MSB	B15	B14	B13	B12	B11	B10	B9	B8	0×00	User Defined Pattern 2 MSB
0×21	Serial Output data control(global)	LVDS output LSB first	SDR/DDR one-lane/two lane, bit wise/bytewise[6:4] 000=SDR two-lane bitwise 001=SDR two-lane bytewise 010=DDR two-lane bitwise 011=DDR two-lane bytewise 100=DDR one-lane			Open	Select 2×frame	Serial output number of bits 00=16 bits 10=12 bits		0×30	Serial stream control.Default causes MSB first and the native bit stream.
0×22	Serial channel status (local)	Open	Open	Open	Open	Open	Open	Channel output reset	Channel power-down	0×00	Used to power down individual sections of a converter.
0×100	Sample rate override	Open	Sample rate override enable	0	0	Open	Sample rate 000=20MSPS 001=40MSPS 010=50MSPS 011=65MSPS 100=80MSPS 101=105MSPS 110=125MSPS			0×00	Sample rate override (requires transfer register,0×FF)
0×101	User I/O Control 2	Open	Open	Open	Open	Open	Open	Open	Open	0×00	Disables SDIO pull-down
0×102	User I/O Control 3	Open	Open	Open	Open	VCM power down	Open	Open	Open	0×00	VCM control
0×109	Sync	Open	Open	Open	Open	Open	Open	Sync next only	Enable sync	0×00	User defined test code 1LSB

MEMORY MAP REGISTER DESCRIPTIONS

Device Index: Register 0x05

There are certain features in the map that can be set independently for each channel,where as other features apply globally to all channels (depending on context)regardless of which are selected.The first four bits in Register 0×05 can be used to select which individual data channels are affected.The output clock channels can be selected in Register 0×05 as well.A smaller subset of the independent feature list can be applied to those devices.

Transfer: Register 0xFF

All registers except Register 0×100 are updated the moment they are written.Setting Bit 0 of this transfer register high initializes the setting in the ADC sample rate override register(Address 0×100).

Power Modes: Register 0x08

Bits[7:6]—Open

Bits 5—External Power-Down Pin Function

If set,the external PDWN pin initiates power-down mode.

If cleared,the external PDWN pin initiates standby mode.

Bits [4:2]—Open

Bits[1:0]—Power Mode

In normal operation (Bits[1:0]),all ADC channels are active.

In power-down mode(Bits[1:0]=01),the digital datapath clocks are disabled while the digital datapath is reset.Outputs are disabled.

In standby mode(Bits[1:0]=10),the digital datapath clocks and the outputs are disabled.

During a digital reset(Bits[1:0]=11),all the digital datapath clocks and the outputs(where applicable)on the chip are reset, except the SPI port,Note that the SPI is always left under control of the user;that is,it is never automatically disabled or in reset (except by power-on reset).

Enhancement Control:Register 0x0C

Bits[7:3]—Open

Bit 2— Chop Mode

For applications that are sensitive to offset voltages and other lowfrequency noise,such as homodyne or direct conversion receivers,chopping translates offsets and other low frequency noise to $f_{CLK}/2$ where it can be filtered.

Bit[1:0]—Open

Output Mode:Register 0x14

Bit7— Open

Bit6— LVDS-ANSI/LVDS-IEEE Option

Setting this bit chooses LVDS-IEEE(reduced range)option.The default setting is LVDS-ANSI.As described in Table9,when LVDS -ANSI or LVDS-LEEE reduced range link is selected,the user can be select the driver termination .The driver current is automatically selected to give the proper output swing.

Table 18.LVDS-ANSI/LVDS-IEEE Option

Output Mode,Bit 6	Output Mode	Output Driver Termination	Output Driver Current
0	LVDS-ANSI	User selectable	Automatically selected to give peoper swing
1	LVDS-IEEE reduced range link	User selectable	Automatically selected to give peoper swing

Bit[5:3]—Open

Bit 2— Output Invert

Setting this bit inverts the output bit stream.

Bit 1— Open

Bit 0 — Output Format

By default,this bit is set to send the data output in twos compleme -nt format .Reseting this bit changes the output mode to offset binary.

Output Adjust:Register 0x15

Bits[7:6]—Open

Bits[5:4]—Output Driver Termination

These bits allow the user to select the internal termination resistor.

Bits[3:1]—Open

Bit 0— Output Drive

Bit 0 of the output adjust rejister control the drive strength on theLVDS driver of the FCO and DCO outputs only,The default values set the drive to 1×while the drive can be increased to 2× by setting the appropriate channel bit in Register0×05 and then setting Bit0.This features cannot be used with the output driver termination select.The termination selection takes precedence over the 2×driver strength on FCO and DCO when both the output driver termination and output driver are selected.

Output Phase:Register 0x16

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

Table 19.Input Clock Phase Adjust Options

Input Clock Phase Adjust,Bits[6:4]	Number of Inputs Clock Cycles of Phase Delay
000(Default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Bits[3:0]—Output Clock Phase Adjust

Table 20.Output Clock Phase Adjust Options

Output Clock Phase Adjust,Bits[3:0]	DCO Phase Adjustment (Degrees Relative to D0±x/ D1±x Edge)
0000	0
0001	60
0010	120
0011(Default)	180
0100	240
0101	300
0111	420
1000	480
1001	540
1010	600
1011	660

Serial Output Data Control:Register 0x21

The serial output data control register is used to programthe MCA9253-125 in various output data modes depending upon the data capture solution .Table21 describes the various serialization options available in the MCA9253-125.

Sample Rate Override:Register 0x100

This register is designed to allow the user to downgrade the device(that is,establish lower power)for applications that do not require full sample rate.Setting in this register are not initalized until Bit0 of the transfer register(Register 0×FF) is set to1.

User I/O Control 2:Register 0x101

Bits[7:1]—Open

Bits 0 —SDIO Pull-down

Bit 0 can be set to disable in the internal 30KΩ pull-down on the SDIO pin,which can be used to limit the loading when many devices are connected to the SPI bus.

User I/O Control 3: Register 0x102

Bits[7:4]—Open

Bit3—VCM Power-Down

Bit 3 can be set high to power down the internal VCM generator. This feature is used when applying an external reference.

Bits[2:0]—Open

Table 21.SPI Register Options

Register 0x21 Contents	Serialization Options Selected				
	Serial Output Number of Bits (SNOB)	Frame Mode	Serial Data Mode	DCO Multiplier	Timing Diagram
0×30	16-bit	1×	DDR two-lane bytewise	4×fs	Figure 2(Default)
0×20	16-bit	1×	DDR two-lane bitwise	4×fs	Figure 2
0×10	16-bit	1×	SDR two-lane bytewise	8×fs	Figure 2
0×00	16-bit	1×	SDR two-lane bitwise	8×fs	Figure 2
0×34	16-bit	2×	DDR two-lane bytewise	4×fs	Figure 3
0×24	16-bit	2×	DDR two-lane bitwise	4×fs	Figure 3
0×14	16-bit	2×	SDR two-lane bytewise	8×fs	Figure 3
0×04	16-bit	2×	SDR two-lane bitwise	8×fs	Figure 3
0×40	16-bit	1×	DDR one-lane	8×fs	Figure 4
0×32	12-bit	1×	DDR two-lane bytewise	3×fs	
0×22	12-bit	1×	DDR two-lane bitwise	3×fs	
0×12	12-bit	1×	SDR two-lane bytewise	6×fs	
0×02	12-bit	1×	SDR two-lane bitwise	6×fs	
0×36	12-bit	2×	DDR two-lane bytewise	3×fs	
0×26	12-bit	2×	DDR two-lane bitwise	3×fs	
0×16	12-bit	2×	SDR two-lane bytewise	6×fs	
0×06	12-bit	2×	SDR two-lane bitwise	6×fs	
0×42	12-bit	1×	DDR one-lane	6×fs	

EQUIVALENT CIRCUITS

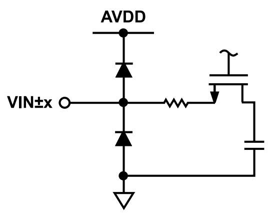

Figure 21. Equivalent Analog Input Circuit

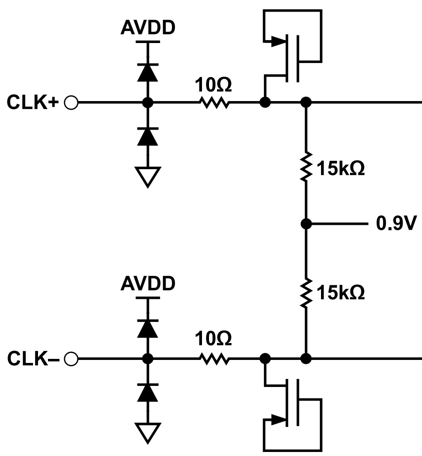

Figure 22. Equivalent CLOCK Input Circuit

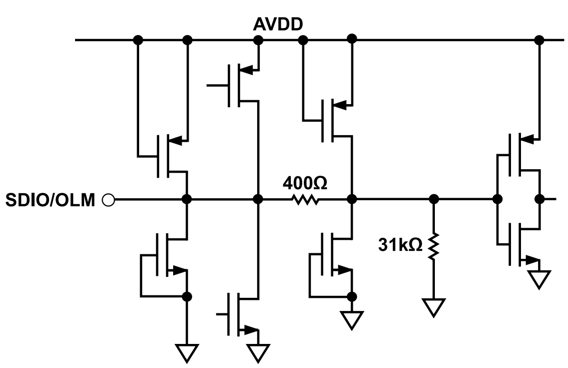

Figure 23. Equivalent SDIO/OLM Input Circuit

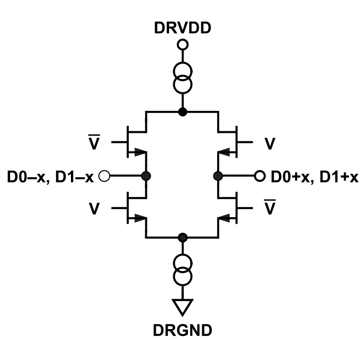

Figure 24. Equivalent Digital Output Circuit

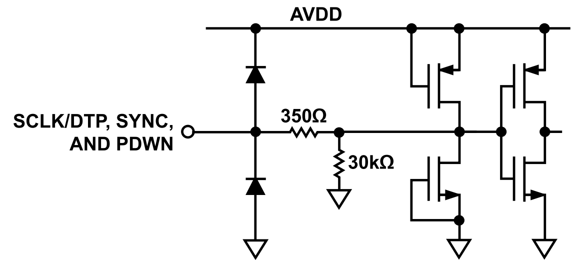

Figure 25. Equivalent SCLK/DTP ,SYNC and PDWN input circuit

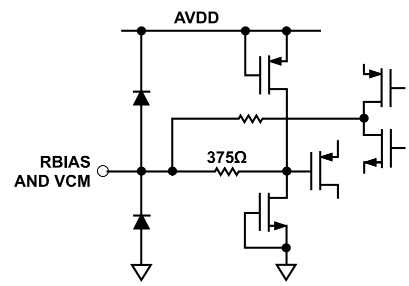

Figure 26. Equivalent RBIAS and VCM Circuit

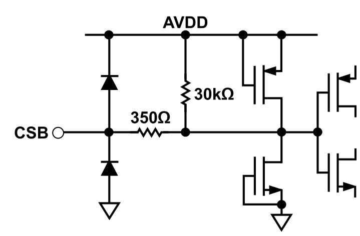

Figure 27. Equivalent CSB Circuit

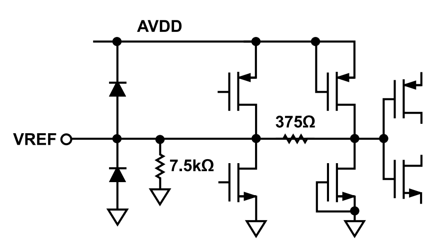

Figure 28. Equivalent VREF Circuit

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the MCA9253 as a systemit is recommended that the designer become familiar with the seguidelines, which describes the special circuit connections and layout requirements that are needed for certain pins.

POWER AND GROUND RECOMMENDATIONS

When connecting power to the MCA9253, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD, several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the MCA9253. With proper decoupling and smart partitioning of the

PCB analog, digital, and clock sections, optimum performance is easily achieved.

EXPOSED PAD THERMAL HEAT SLUG RECOMMENDATIONS

It is required that the exposed pad on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the MCA9253. An exposed continuous copper plane on the PCB should made to t -he MCA9253 exposed pad, Pin 0.The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous copper plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the ADC and PCB during the reflow process, where as using one continuous plane with no partitions only guarantees one tie point. See Figure 29 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at www.analog.com.

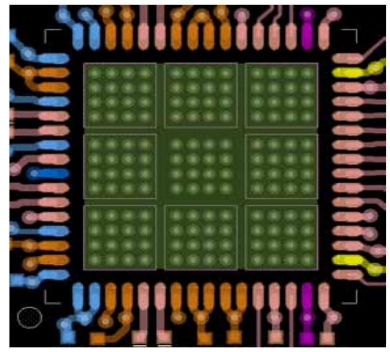

Figure 29.Typical PCB Layout

VCM

The VCM pin must be decoupled to ground with a 0.1uF capacitor.

REFERENCE DECOUPING

The VREF pin must be externally decoupled to ground with a low ESR,1.0uF capacitor in parallel with a low ESR,0.1uF ceramic capacitor.

SPI PORT

The SPI port must not be active during periods when the full dynamic performance of the converter is required.Because the SCLK,CSB,and SDIO signals are typically asynchronous to the ADC clock,noise from these signals can be degrade converter performance.If the on-board SPI bus is used for other devices,it may be necessary to provide buffers between this bus and the MCA9253-125 to keep these signals from transitioning at the converter inputs during ciritcal sampling periods.

CROSSTALK PERFORMANCE

The MCA9253-125 is available in a 48-lead VQFN package with the input pairs on the either corner of the chip.See for the Figure 9 for the pin configuration.To maximize the crosstalk performance on the board,add grounded filled vias in between the adjacent.

OUTLINE DIMENSIONS

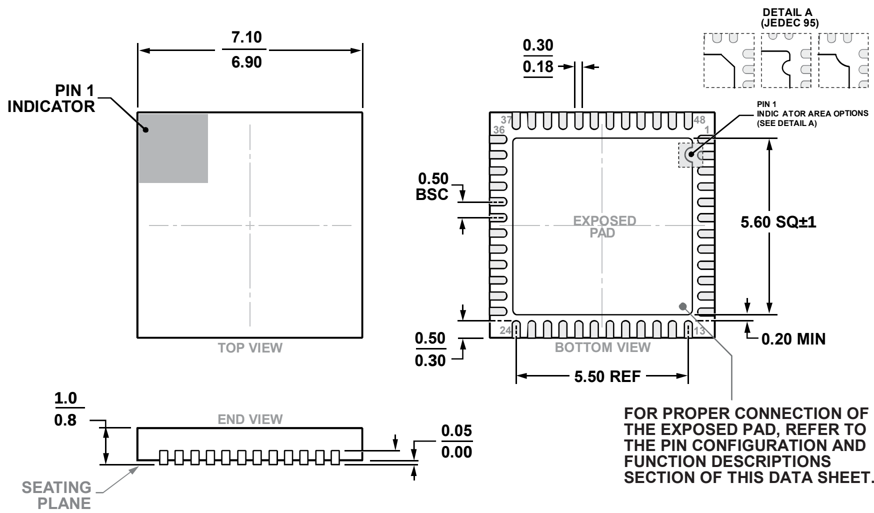

Figure 3 0 . 48-Lead VQFN
Dimensions shown in millimeters

ORDERING INFORMATION

Model[1]	Temperature Range	Package Description	Packaging Quantity
MCA9253-125	−40°C to +85°C	48-Lead VQFN	

Note[1]:Z=RoHS Compliant Part.

Version	Update Details
V1.0	Initial Version
V2.0	Supplement Register configuration