MCDCM4615

Dual-Channel 6A DC/DC Converters & Single 1.5A LDO Regulator

Features

DC/DC Section:

- Input Voltage Range: 4.5V-5.5V
- Adjustable Output Voltage: 1.0V-3.3V
- Output Current: Dual 6A or Single 12A
- Voltage Regulation: 0.5% (Typ.)
- Load Regulation: 0.5% (Typ.)
- Multi-phase Parallel Current Sharing
- Current Mode Control, Fast Transient Response
- PGOOD Function
- Soft Start/Output Voltage Tracking
- Overcurrent, Short-Circuit, and
- Overtemperature Protection

LDO Section

- Input Voltage Range: V_{LDO-IN} = 1.6V-3.6V
- VCNTL: 4.5V-5.5V
- Output Voltage Range: $V_{LDO-OUT}$ = 0.8V-3.5V
- Output Current Range: I_{OUT} = 0-1.5A
- BGA Package: 15mm × 15mm × 3.42mm

Applications

- FPGA/DSP Power Supply
- Multi-Voltage Rail Systems

Description

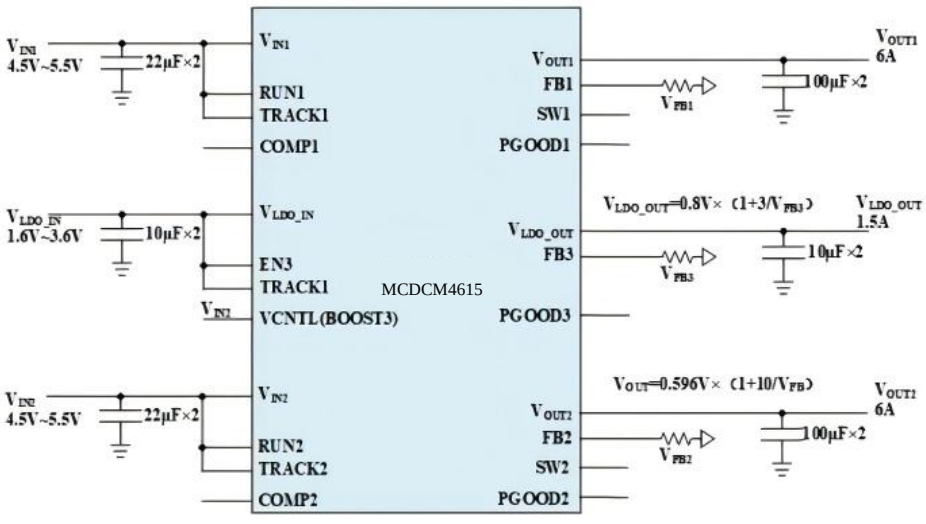
The MCDCM4615 is a triple-output power module that includes a 1.5A output LDO (Ultra-Low Dropout) linear regulator and dual 6A output switching-mode DC/DC power supplies. The package integrates switching controllers, inductors ,a 1.5A regulator, and all supporting components. The dual 6A DC/DC converters operate over an input voltage range of 2. 7V to 5.5V, while the LDO operates within an input voltage range of 1.1V to 5.5V. The MCDCM4615 supports an adjustable output voltage range of 1.0V to 3.3V (for the DC/DC converters) and 0.8V to 3.5V (for the LDO). The output voltage for each channel is set via an external resistor, requiring only bulk capacitors at the input and output.

This circuit is a critical component of the overall system, ensuring reliability and stable operation. Therefore, the power supply is designed for high reliability and long lifespan.

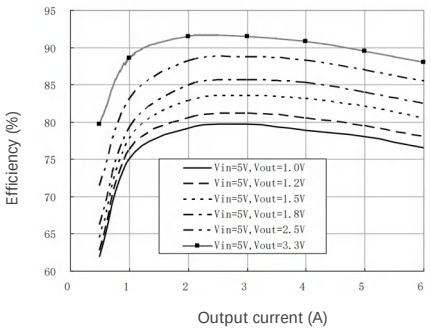
As a surface-mount module, the MCDCM4615 is assembled onto PCBs using reflow soldering. It features a compact size, high integration, and lightweight design.

Typical applicaTion

Two-channel independent operation mode typical application circuit



5V Input Load Efficiency Curve



AbsoluTe Maximum Ratings Note1

DC/DC Section:

V_{IN},SV_{IN}(per channel)..... 2.7V-5.5V

V_{OUT}(per channel).....0.6V-5V

Output Current Range

I_{OUT}.....0-8A (single-channel standalone operation)

LDO Section

Input Voltage Range

V_{LDO-IN}.....0-5.5V

Input Power Voltage

VCNTL=V_{IN}.....4.5V-5.5V

Output Voltage Range

$V_{LDO-OUT}$.....0.8-5.5V

Output Current Range

I_{OUT}.....0-2A

Pin Soldering Temperature Resistance..250°C (30s)

Storage Temperature Range(T_{sig})... - 55°C to 125°C

Note 1: Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. Extended operation under absolute maximum conditions may affect device reliability and lifespan.

Note 2: High-temperature derating must be considered during operation. Case temperature (T_C) ≤ 125°C.

Recommended Operating Conditions

DC/DC Section:

Input Power Voltage

V_{IN}.....4.5V-5.5V

Output Voltage Range

V_{OUT}.....1.0-3.3V

Output Current Range

I_{OUT}....0-6A (single-channel standalone operation)

LDO Section

Input Voltage Range

V_{LDO-IN}.....0-5.5V

Input Power Voltage

V_{CNTL}=V_{IN}.....4.5V-5.5V

Output Voltage Range

$V_{LDO-OUT}$.....0.8-5.5V

Output Current Range

I_{OUT}.....0-2A

Operating Case Temperature(YC)(Note2).....

-40°C to 125°C

PCB Soldering Profiles

Typical Leaded Profile

Peak Temperature.....210°C-230°C

Liquidus Time.....30s-90s

Typical Lead-Free Profile

Peak Temperature.....240°C-250°C

Liquidus Time.....30s-90s

Thermal Resistance

Model	Package	Dimensions (mm)	Test Board Size (mm)	Junction-to-Ambient θ_{JA}	Junction-to-Substrate $\theta_{JCbottom}$	Junction-to-Top θ_{JCtop}
MCDCM4615	BGA	15×15×3.42	100×100 (4-layer)	15.5°C/W	2.7°C/W	25°C

PIN Configuration

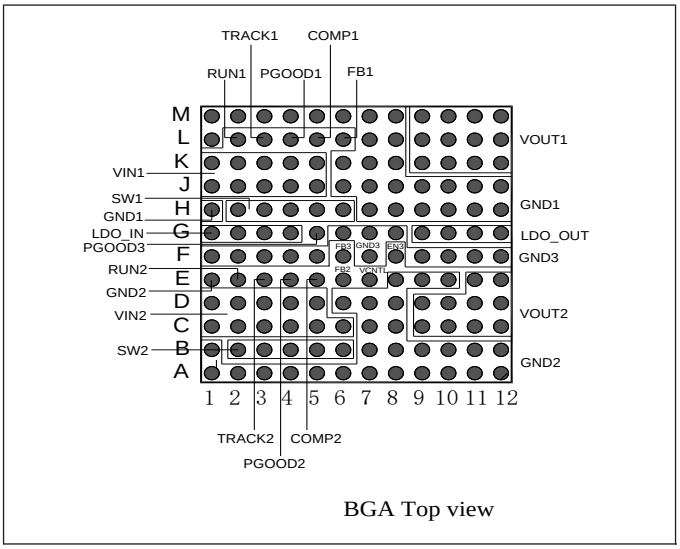


Figure 1. Pin defines the top view

PIN	Definition	Pin Description
J1-J5，K1-K5	V_{IN1}	Power input pins for each channel. Connect filter capacitors directly between the input and ground.
C1-C6，D1-D5	V_{IN2}	
H1，H7-H12，J6-J12，K6-K8，L1，L7-L8，M1-M8	GND1	Power ground for input and output loops of each channel.
A1-A12，B1，B7-B12，C7-C8，D6-D8，E1，E8-E10	GND2	
H1，H7-H12，J6-J12，K6-K8，L1，L7-L8，M1-M8	GND1	Power ground for input and output loops of each channel.
A1-A12，B1，B7-B12，C7-C8，D6-D8，E1，E8-E10	GND2	
L3	TRACK1	Output voltage tracking terminal for each channel. Connect a resistor and capacitor to TRACK to extend soft-start time. If unused, connect to V_{IN}; do not leave floating.
E3	TRACK2	
L6	FB1	Inverting input of the error amplifier for each channel. Internally connected to V_{OUT} via a 10k precision resistor. Set output voltage by connecting an external resistor between FB and GND.
E6	FB2	
F6	FB3	Inverting input of the LDO error amplifier. Internally connected to V_{LDO_OUT} via a 3k precision resistor.
L5	COMP1	Current control threshold and error amplifier compensation point. For parallel operation, connect COMP pins of all channels to enable current sharing.
E5	COMP2	
L4	PGOOD1	Open-drain logic output indicating channel status. Pulls low if output voltage deviates by ±10% from the set value.
E4	PGOOD2	

PIN	Definition	Pin Description
L2	RUN1	Enable control pin. The module operates when the pin voltage exceeds 1.5V.
E2	RUN2	
H2-H6	SW1	Switching node for circuit testing purposes.
B2-B6	SW2	
G1-G4	LDO_IN	LDO input pin.
G9-G12	LDO_OUT	LDO output pin.
E7	VCNTL	Boost supply for driving the internal LDO MOSFET to full enhancement. Ensure VCNTL - VLDO_OUT > 1.7V. When VCNTL is externally connected to 5V, the LDO achieves lower dropout voltage. Internally connected to VIN2. Both LDO_IN and VIN must be present during operation.
F1-F5，F7，F9-F12，G6-G8	GND3	Power ground for the input and return paths of the internal LDO.
G5	PGOOD3	Open-drain logic output indicating LDO status.
F8	EN3	LDO enable pin.

Electrical Characteristics

Symbol	Parameter	Test Condition (Note 3)	Limits			Unit
			Min	Typ	Max	
DC/DC Section						
V_{IN1}，V_{IN2}	Input DC Voltage	—	3.3	—	5.5	V
V_{OUT1}，V_{OUT2}	Output Voltage	C_{IN}=22μF×2，C_{OUT}=100μF×2 V_{IN}=3.3V~5.5V， R_{FB}=6.65kΩ I_{OUT}= 0A~6A	1.474	1.500	1.526	V
$V_{IN1(ULVO)}$,$V_{IN2(ULVO)}$	Input Undervoltage Threshold	I_{OUT}=0A	1.85	2.0	2.35	V
I_Q(V_{IN1} ,V_{IN2})	Quiescent Current	V_{IN}=5V，V_{OUT}=1.5V	—	62	—	mA
I_S(V_{IN1} ,V_{IN2})	Input Supply Current	V_{IN}=5V，V_{OUT}=1.5V，I_{OUT}=6A	—	2.2	—	A
$I_{OUT1(DC)}$ $I_{OUT2(DC)}$	Output Current	V_{OUT}=1.5V，V_{IN}=5V	0	—	6	A
S_{V1} S_{V2}	Voltage Regulation	V_{OUT}=1.5V， 0A V_{IN} =3.3V~5.5V	—	0.5	1.5	%
S_{I1} S_{I2}	Load Regulation	V_{OUT}=1.5V， 0A~6A V_{IN}=5V	—	0.5	1.5	%
V_{pp1} V_{pp2}	Output Ripple Voltage	I_{OUT}=0A， C_{OUT}≥200μF V_{IN}=5V，V_{OUT}=1.5V	—	30	50	mV_{P-P}
f_{S1} f_{S2}	Switching Frequency	V_{OUT}=1.5V, I_{OUT}=6A，V_{IN}=5V	1.25	1.5	1.75	MHz
△$V_{OUT1(LS)}$ △$V_{OUT2(LS)}$	DynamicResponse	Load: 0%~50%~0% C_{OUT}=200μF V_{IN}=5V，V_{OUT}=1.5V	—	100	—	mV
$t_{SETTLE1}$ $t_{SETTLE1}$	Dynamic Recovery Time	Load: 0%~50%~0% V_{IN}=5V，V_{OUT}=1.5V	—	20	—	μS
$I_{OUT1(PK)}$ $I_{OUT2(PK)}$	Output Current	C_{OUT}=100μF，V_{IN}=5V，V_{OUT}=1.5V	—	14	—	A
V_{FB1},V_{FB2}	FBPin Voltage	V_{OUT}=1.5V，I_{OUT}=0A	0.590	0.596	0.602	V
V_{LDO-IN}	Operating Voltage	V_{CNTL} -$V_{LDO-OUT}$＞1.7V	1.1	—	5.5	V
V_{BOOST3}	V_{CNTL} Voltage	—	4.5	5	5.5	V
V_{FB3}	FB3 Internal Reference Voltage	1mA≤I_{OUT}≤1A，1.6V≤V_{LDO_IN}≤5.5V V_{CNTL} =5V，1V≤V_{OUT}≤3.5V	0.792	0.8	0.808	V
$V_{LDO-OUT}$	Output Voltage Range	—	0.8	—	3.5	V
V_{DO}	Dropout Voltage	V_{CNTL} -$V_{LDO-OUT}$＞1.7V	—	240	—	mV
I_{OUT}	Output Current	V_{EN3}≥0.8V	—	—	1.5	A
V_{RUN1}，V_{RUN2}	Enable Threshold	RUN Rising	1.4	1.5	1.7	V

Note 3: Electrical parameter testing results are based on the module soldered onto the evaluation board.

Product Principle Block Diagram

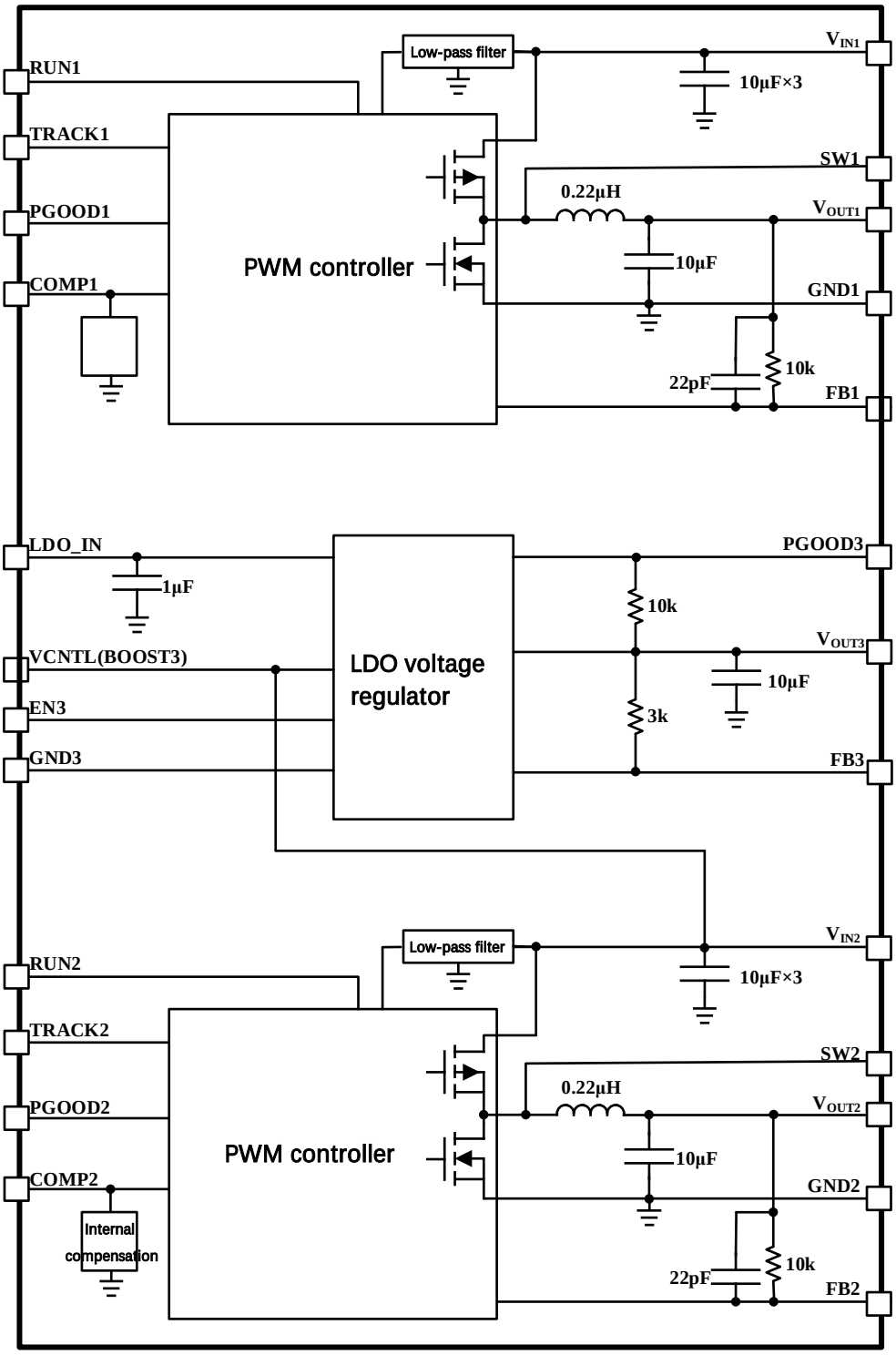


Figure 2. Block diagram of the principle of MCDCM4615

Typical Performance Characteristics

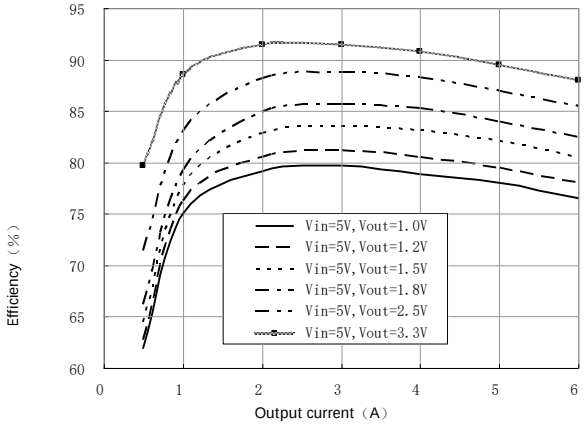


Figure 3. 5V input-load-efficiency curve

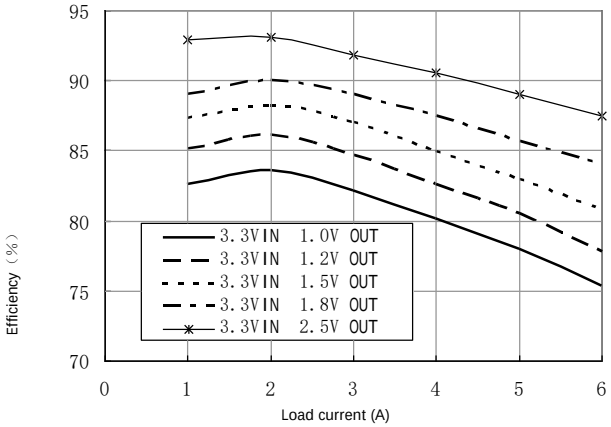
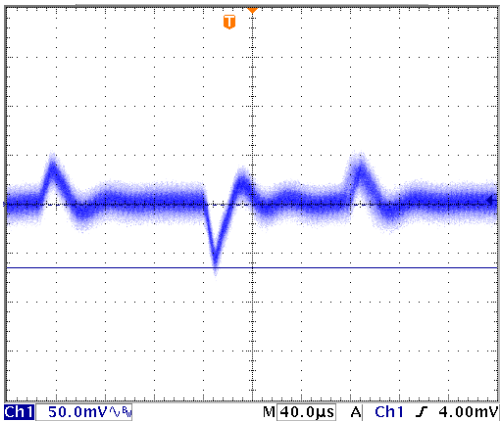


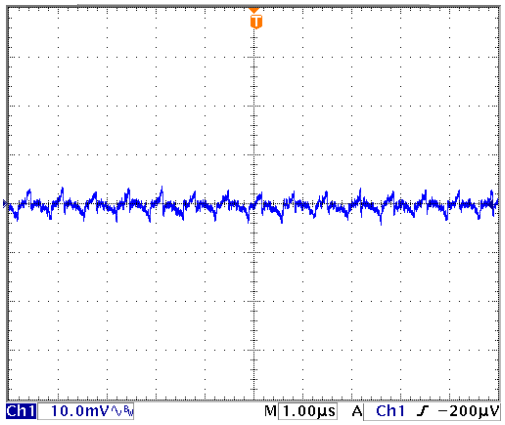
Figure 4. 3.3V input-load-efficiency curve



V_{IN}=5V； V_{OUT} =1.5V； I_{OUT} =0~2A~0；

f=1kHz（T=1ms）； C_{OUT} ≥100μF×2

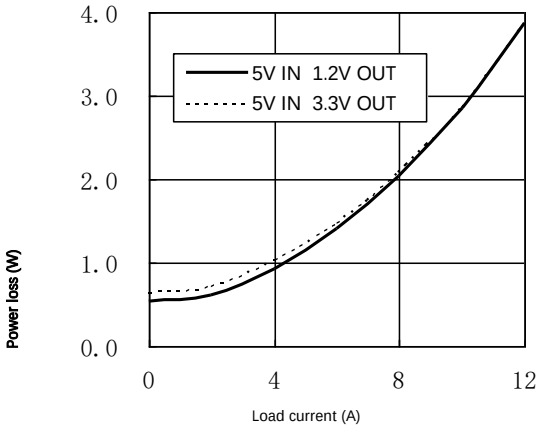
Figure 5. Load-dynamic curve



V_{IN}=5V； V_{OUT} =1.5V； I_{OUT} =6A；BW：20MHz

C_{OUT} ≥100μF×2

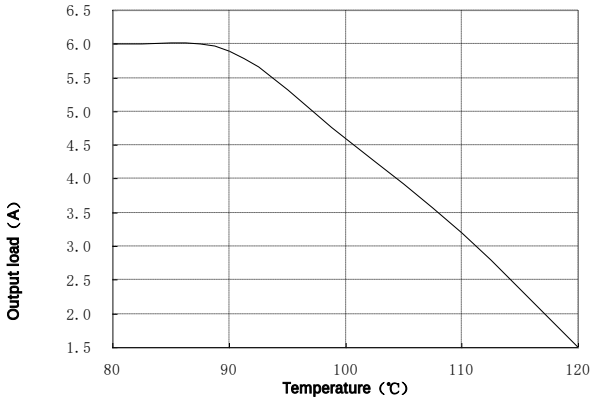
Figure 6. Output ripple voltage



V_{OUT} =1.2V、3.3V； I_{OUT}=0~12A;

Dual-path parallel connection

Figure 7. Load-power consumption relationship curve



V_{IN}=5V，V_{OUT}=1.5V，T_C≤125℃，IOUT=0~6A；T_S：≤125℃

Dual DC/DC channels operate simultaneously

Figure 8. Demotion curve

Applications Information

Switching Regulator Section

The MCDCM4615 is a dual-channel, non-isolated switching-mode DC/DC power supply. Each channel can deliver up to 8A of DC output current with minimalexternal input and output capacitors. Within an input voltage range of 3.3V–5.5V, the module provides two tightly regulated outputs (adjustable from 0.6V to 5V via an external resistor). A typical application schematicis shown in Figure 11.

The MCDCM4615 integrates two constant-frequency, current-mode regulators with high-speed power MOSFETs. The typical switching frequency is 1.5MHz.

Through current-mode control and internal feedback loop compensation, the MCDCM4615 module provides sufficient stability margin and excellent transient performance, while supporting a wide range of output capacitors, including all-ceramic capacitors.

Current-mode control offers over-current protection and over-temperature protection under fault conditions. When the output feedback voltage exceeds ±10% of the set value, the internal over-voltage and under-voltage comparators will pull the open-drain PGOOD output low.

Pulling any RUN pin below 1.3V forces the corresponding regulator into shutdown state. The TRACK pin is used to configure soft-start functionality during startup and voltage tracking.

The MCDCM4615 employs internal compensation to maintain stability under all operating conditions. The FB pin sets the output voltage by connecting to ground through an external resistor.

A typical application circuit for the MCDCM4615 is shownin Figure 11. The selection of external components is primarily determined by the maximum load current and output voltage requirements.

VLDO Section

The VLDO (Ultra-Low Dropout) linear regulator operates with an input voltage range of 1.6V to 3.6V. The VLDO utilizes an internal NMOS transistor as a passdevice configured in a source follower setup. VCNTL is internally connected to VIN2 within the module, providing bias voltage for the LDO path.

The LDO delivers a high-accuracy output capable of supplying 1.5A current with a typical dropout voltage of 100mV. Two 10μF ceramic capacitors are sufficient to fully meet the output capacitor bypass requirements. The low reference voltage enables the V_{LDO} to maintain a lower output voltage compared to conventional LDOs.

Additionally, the device incorporates current limiting and thermal overload protection features. The NMOS follower architecture ensures fast transient response characteristics.

V_{IN}-to-V_{OUT} Step-Down Ratio

For a given input voltage on the two switching regulators, the maximum achievable step-down ratio from V_{IN} to V_{OUT} is limited. The minimum V_{IN} -to-V_{OUT} voltage drop of the MCDCM4615 is a function of the load current. With a 5V input voltage, both regulators can deliver 6A current for outputs up to 3.3V.

Output Voltage

Each regulator controller has an internal 0.596V reference voltage. As shown in the block diagram, a 10kΩ internal feedback resistor connects V_{OUT} to the FB pin. An external resistor R_{FB}, placed between the FB and GND pins, sets the output voltage:

$$R_{FB} = \frac{0.596V}{V_{OUT} - 0.596V} \times 10k$$

Table 1: Output Voltage vs. R_{FB} Resistance Values

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3
R_{FB} (kΩ)	Open	14.75	10	6.65	4.87	3.09	2.21

For parallel operation of NN channels:

$$R_{FB} = \frac{0.596V}{V_{OUT} - 0.596V} \times \frac{10k}{N}$$

Input capacitor

The MCDCM4615 module should be connected to a low AC impedance DC power supply. For each

voltage regulator channel, it is recommended to use two 22μF ceramic input capacitors to achieve RMS ripple current decoupling. Only when there are long inductive wires or traces at the input end, a large-capacity input capacitor is required. This large-capacity capacitor can be an aluminum electrolytic capacitor or a solid-state capacitor.

If inductor current ripple is neglected, the RMS current of the input capacitor can be estimated using the following formula:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\,\%} \times \sqrt{D \times (1-D)}$$

Where η% is the estimated efficiency of the power module.

Output Capacitor

The MCDCM4615 switching power supply is designed to achieve low output voltage ripple on each channel. The output capacitor must have sufficiently low effective series resistance (ESR) and high capacitance to meet ripple and transient requirements. Suitable capacitors include low-ESR aluminum capacitors, low-ESR polymer capacitors, or ceramic capacitors. A typical configuration uses ≥200μF ceramic capacitors. For further reduction of output ripple or transient peaks, additional filtering (e.g., parallel capacitors such as 1μF, 0.1μF, or 1000pF) may be required to suppress high-frequency noise. Output filter capacitors must be tightly connected to the power loop (refer to the PCB layout diagram). Multiple vias should be placed to interconnect power layers for optimal filtering.

Output Voltage Tracking

Output voltage tracking can be externally programmed using the TRACK pin. The output of a slave converter can track and follow the master converter. The master converter's output is divided by an external resistor divider, which matches the feedback divider of the slave converter for synchronized tracking. The MCDCM4615 internally uses a precision 10kΩ resistoras the upper divider for output sampling.Figure 13 illustrates an example of output tracking.

$$\text{Slave} = (1 + \frac{10k}{R_{TA}}) \times V_{TRACK}$$

V_{TRACK} is the ramp applied to the slave converter's output. The control range of V_{TRACK} is 0V to 0.596V, corresponding to the internal reference voltage. When the main output uses the same setting resistance value as the slave output, the slave output will be consistent with the main output until it reaches the final value. Starting from the adjustment point of the slave output, the main output will continue to reach the final value. When V_{TRACK} is greater than 0.596V, voltage tracking is disabled. In Figure 9, R_{TA} will be equal to the R_{FB} of the overlapping tracking. The startup of the main output can be controlled by an external ramp or by R_{SR} and C_{SR} referenced to V_{IN} in Figure 9. The ramp time can be programmed using the following formula:

$$t = -\left(\ln\left(1 - \frac{0.596V}{V_{IN}}\right) \times R_{SR} \times C_{SR}\right)$$

The output slope (MR) of the main voltage regulator and the output slope (SR) of the subordinate voltage regulator, expressed in terms of "output voltage/time", are determined by the following formula:

$$\frac{MR}{SR} \times 10k = R_{TB}$$

Here, MR denotes the primary output conversion rate, and SR denotes the secondary output conversion rate, with units of volts per time. When continuous tracking is required, MR equals SR, resulting in R_{TB} being set to 10k. R_{TA} can then be determined using the following formula:

$$R_{TA} = \frac{0.596V}{\frac{V_{FB}}{10k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

Here, V_{FB} denotes the feedback voltage reference of the regulator, and V_{TRACK} is set to 0.596V. During the overlap tracking process, R_{TB} corresponds to the 10k top feedback resistor of the regulator. Consequently, R_{TA} is equivalent to R_{FB2}, which aligns with both V_{FB} and V_{TRACK}.

Therefore, in Figure 9, R_{TB} = 10k and RTA = 6.65k. Figure 9 shows the output voltage of the overlapping tracking.

In the output voltage tracking, a different conversion rate may be required from the regulator. When SR is slower than MR, R_{TB} can be set to ensure that the conversion rate from the output is fast enough to reach the final value from the output voltage before the main output.

For example: MR = 3.3V/ms and SR = 1.5V/ms. Then R_{TB} = 22.1k. Solving for R_{TA} gives 4.87k.

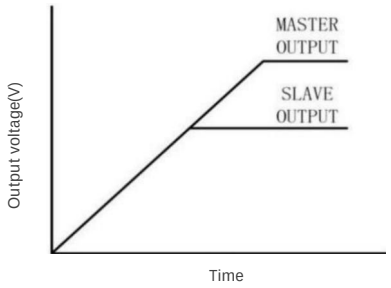


Figure 9. Schematic diagram of coincident tracking

PGOOD Function

The PGOOD pin is an open-drain pin used to indicate whether the output voltage is within the normal range. This pin monitors theoutput voltage for deviations within ±10% of the set value. Since the PGOOD pin cannot actively drive a high level, an external pull-up resistor is required. It is recommended to connect the pull-up resistor to the respective channel's VIN pin, witha resistance value configurable between 10kΩ and 100kΩ.

Enable Function

The RUN pin serves as the enable control for the switching-mode DC/DC converter in each channel. When the RUN pin is pulled below 1.5V, the MCDCM4615 enters a shutdown state. Applying a voltage above 1.5V to the RUN pin activates the power stage and enables normal operation.

COMP Pin

This pin is designated for external compensation.The module is internally compensated for all output voltage configurations. During parallel operation, the COMP pins of all channels must be connected together to ensure proper functionality.

VLDO Section

Adjustable Output Voltage

The output voltage is set by the ratio of two resistors . A 3kΩ resistor is internally connected between LDO _OUT and FB3. An additional resistor (R_{FBLDO}) must beplaced between FB3 and GND3 to set the output voltage within the range of 0.8V to 3.5V.

Formula:

$$R_{FBLDO} = \frac{0.8V}{V_{LDO\_OUT} - 0.8V} \times 3k$$

Power Supply Operation

The VLDO incorporates a delayed open-drain PowerGood (PGOOD3) pin. When the VLDO is in shutdown mode or under-voltage lockout (UVLO) state, the PGOOD3 pin exhibits a low impedance to ground. As the output voltage of the VLDO rises to 90% of its nominal stable voltage, the PGOOD3 transitions to a high-impedance state. The PGOOD3 pin will remain in this high-impedance state until the output voltage drops below 90% of its nominal stable voltage. A pull-up resistor can be connected between the PGOOD3 pin and a positive logic power supply (e.g., VLDO output or input). To ensure proper functionality of the Power Good circuit, LDO_IN must be at least 1.6V or higher.

Output Capacitor and Transient Response

The VLDO remains stable with a wide range of ceramic output capacitors. The stability is influenced by the capacitor's ESR, particularly for capacitors with higher ESR values. To ensure stability, it is recommended to use two or more 10μF (or larger) output capacitors. Larger capacitors can reduce transient deviations under load variations. While bypass capacitors on the load side increase the effective output capacitance, high-ESR electrolytic

capacitors may be used, but they must be paralleled with a ceramic capacitor at the output.

Overtemperature Protection

The internal overtemperature protection circuit monitors the junction temperature of the module. If the junction temperature reaches approximately 150°C, both power switches will be disabled until the temperature decreases by about 25°C.

Recommended PCB Layout

1.Pad Design

BGA pad diameter: 0.63mm (recommended).
Adjust solder mask openings for high-power pins (e.g., VIN, GND, VOUT) to ensure uniformity. If not optimized, PCB manufacturers may apply default solder mask openings (~0.1mm), leading to inconsistent pad sizes. Mismatched openings can cause uneven solder tension during reflow, potentially squeezing or stretching adjacent solder joints.

2. PCB Layout

To optimize the electrical and thermal performance of the PCB layout, the following considerations should be implemented:
a. For high-current paths, allocate large copper foil areas on the PCB, including VIN, GND, and VOUT. This approach effectively reduces conduction losses and alleviates thermal stress on the PCB.
b. Position high-frequency ceramic capacitors in close proximity to the VIN, GND, and VOUT pins to mitigate high-frequency noise.
c. Place a dedicated power layer beneath the module;
d. To minimize through-hole conduction losses and reduce module thermal stress, multiple through-holes can be used to connect the top layer and other power layers;
e. Do not layout the through-holes directly on the pads, unless the through-holes are filled;
f. For parallel modules, connect the pins COMP, V_{FB}, RUN, and TRACK together.

Figure 10 provides a recommended PCB board layout.

3. Recommended Solder Pad

For the MCDCM4615 product, the typical diameter of the BGA solder balls is 0.76mm. It is recommended that users design the BGA packag library according to the dimensions shown in Table 2.

Table 2. Recommended Pad Dimensions for MCDCM4615

Part Number	BGA Ball Diameter (mm)	Recommended Pad Opening Size (mm)
MCDCM4615	0.76	Φ0.63

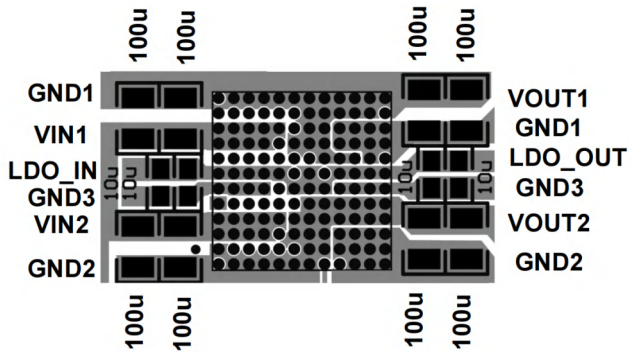


Figure 10. Recommended PCB layout for MCDCM4615

Safety Precautions

The MCDCM4615 module does not provide electrical isolation between V_{IN} and V_{OUT}. If required, install a slow-blow fuse rated for twice the maximum input current to protect the device from catastrophic failure. The module includes thermal shutdown and overcurrent protection features.

Typical application diagram

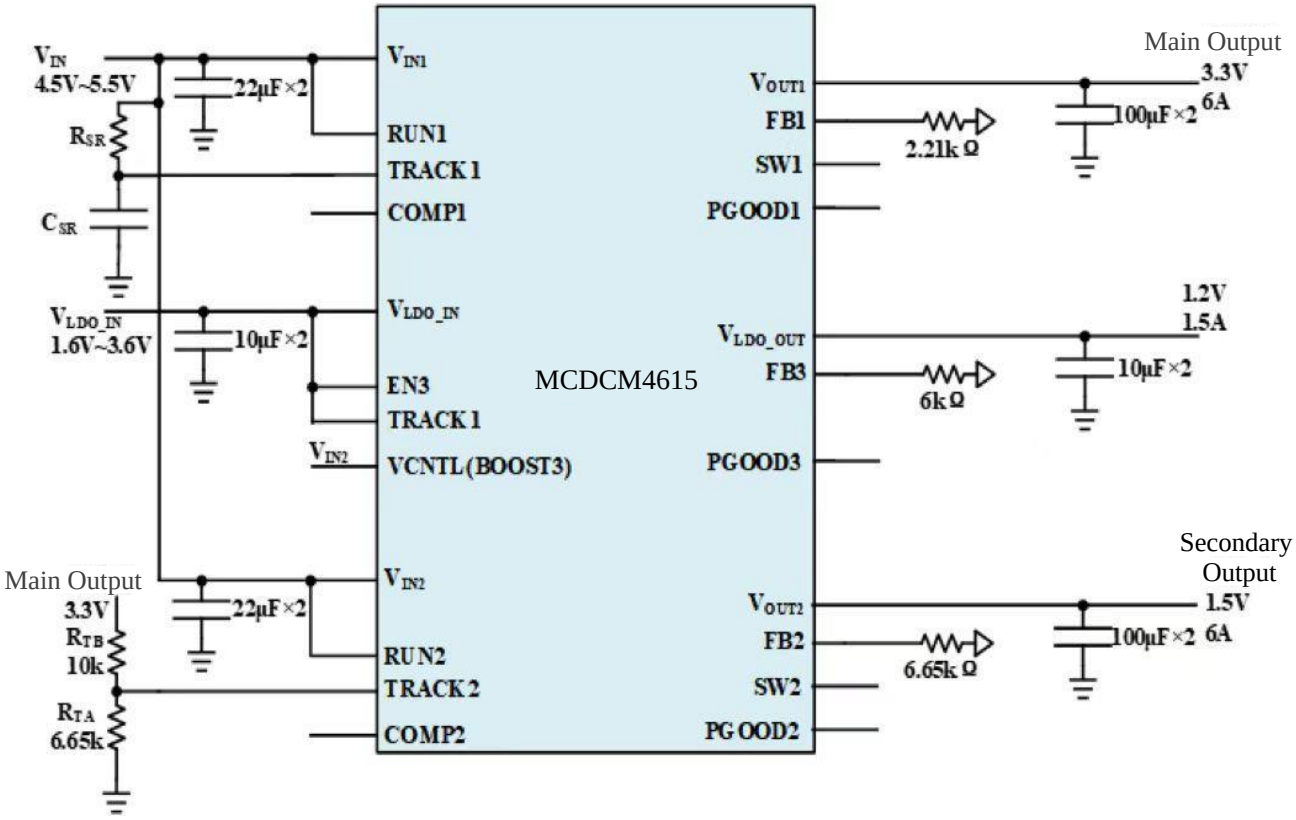


Figure 11. Single-path DC/DC output 1.5V, load 6A; LDO output 1.2V, load 1.5A

(VCNTL has been internally connected to the V_{IN} pin. It can be left unconnected externally, and the same applies below.)

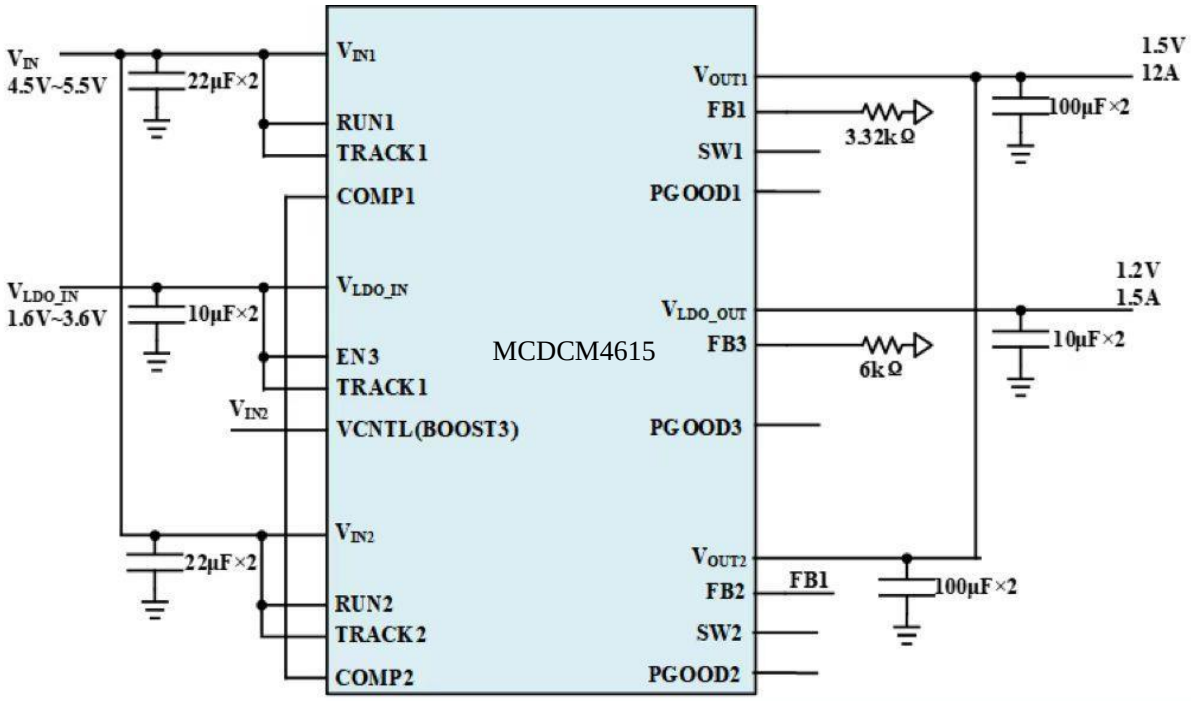


Figure 12. Parallel DC/DC output 1.5V, load 12A; LDO output 1.2V, load 1.5A

Typical application diagram

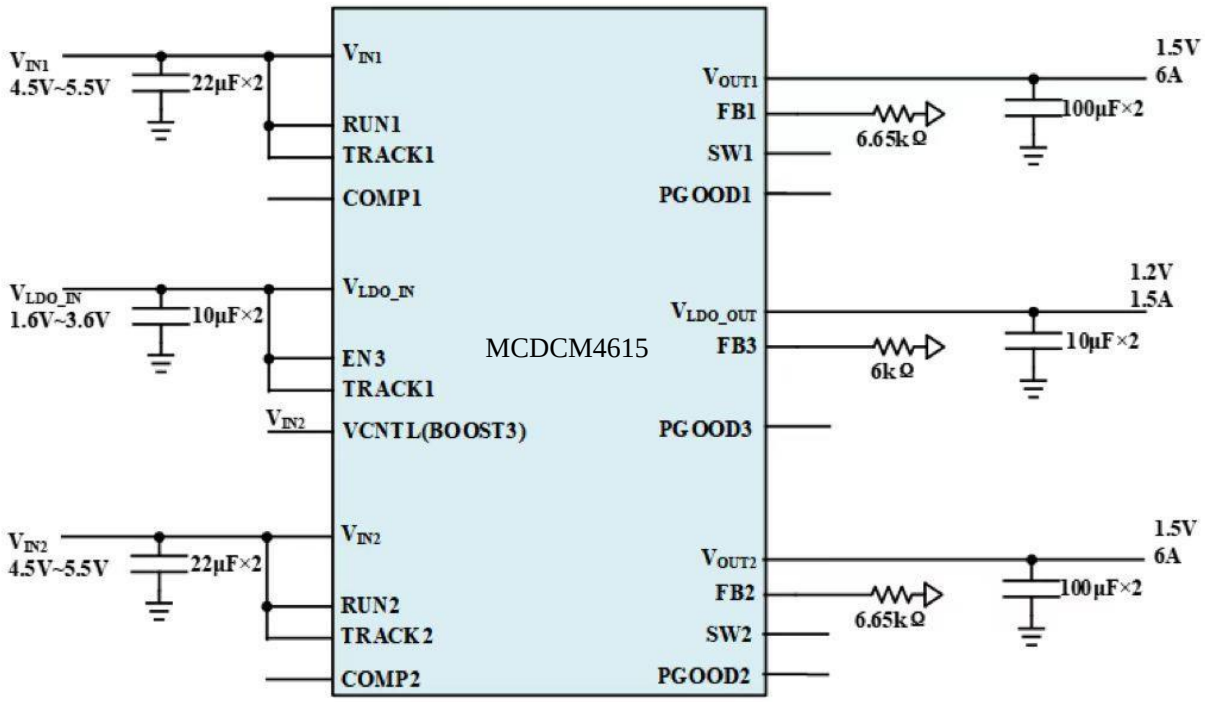
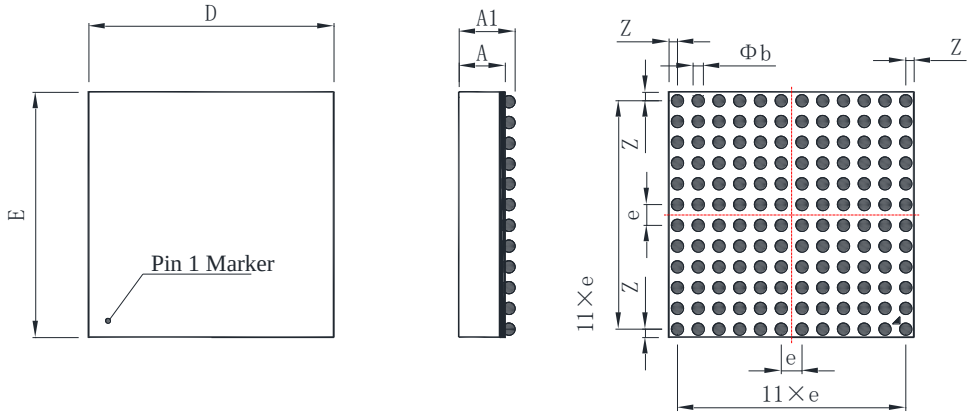


Figure 13. Dual-output DC/DC module providing 3.3V and 1.5V, achieving overlapping tracking; LDO outputting 1.2V with a load of 1.5A

Product Size

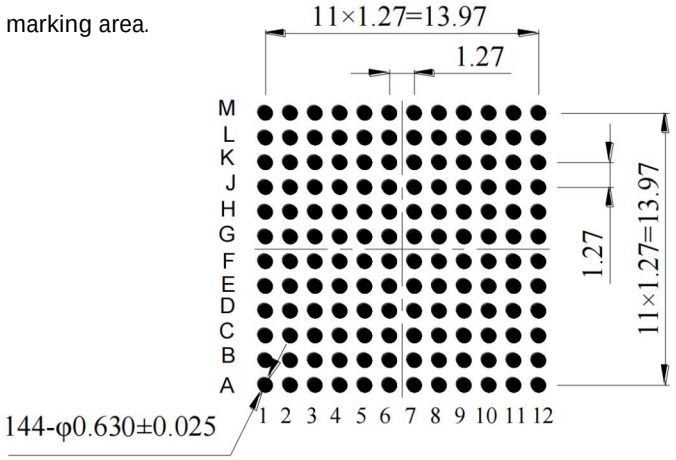


Unit: mm

Dimension Symbol	Value		
	Min	Nominal	Max
A	-	2.82	3.00
A1	-	3.42	3.60
D	14.80	15.00	15.20
E	14.80	15.00	15.20
Φb	0.66	0.76	0.86
e	1.12	1.27	1.24
Z	-	0.52	0.67

Figure 14. Dimensions of MCDCM4615

Note◢ indicates the first terminal marking area.



BGA Pakage

Figure 15. Recommended Pad Dimensions for PCB

Electronics Assembly Instructions

Storage Requirements

General Requirements: Plastic encapsulated products (devices) must be stored in a clean, ventilated, non-corrosive environment equipped with temperature and relative humidity monitoring instruments. Plastic encapsulated products (devices) are shipped in anti-static sealed packaging. If the package is opened and the products are not assembled within 168 hours, they must be re-sealed in anti-static bags using vacuum sealing for storage .

Storage Conditions: Storage temperature: 10°C to 25°C; relative humidity: ≤70% RH; valid storage period: 18 months.

Recommended Environmental Process Conditions

1. Product Pre-Treatment

For plastic-encapsulated modules: pre-bake at 125° C for 48 hours before use, or follow IPC/JEDECJ-STD-033B *"Handling, Packaging, Shipping, and Use of Moisture/Reflow-Sensitive Components"* to ensure moisture removal. Complete reflow soldering within 48 hours after baking.

2. Soldering Materials

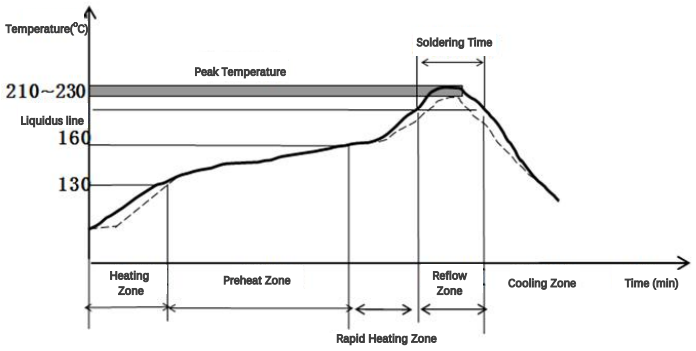
For lead-based soldering, it is recommended to use lead-based solder paste compositions such as Sn63Pb37 or Sn62Pb36Ag2. For lead-free soldering , the use of lead-free solder paste, specifically Sn96. 5Ag3Cu0.5, is advised. The solder paste should comply with a grade of 3 or higher.

3. Component Placement

The center of the module pad should be aligned with the printed solder paste. If the stencil thickness is 0.13 mm, the module pad should be pressed into the solder paste to a depth of approximately 0.05 mm. If the pick-and-place machine allows pressure adjustment, ensure the pressure is sufficient to maintain good contact between the pad and solder paste, but not excessive enough to squeeze the solder paste onto the solder mask outside the pad. Proper contact with the solder paste minimizes voids to the greatest extent, and solder voids must not exceed 25%.

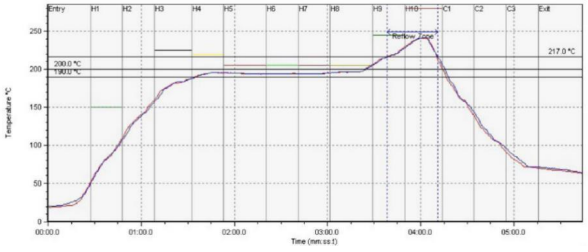
4. Recommended Reflow Profiles

The module is compatible with both lead-based (see Figure 16) and lead-free (see Figure 17) reflow profiles . Use a 9-zone or higher reflow oven to ensure uniform temperature distribution(Note4



No.	Item	Condition
1	Maximum temperature rise slope in preheat zone	≤3°C/s
2	Maximum temperature drop slope in preheat zone	≤4°C/s
3	Preheat zone duration (130~160°C)	60s~120s
4	Peak temperature in reflow zone	210°C~230°C
5	Reflow zone duration (time ≥183°C for Sn63Pb37)	30s~90s

Figure 16. Typical lead-based reflow soldering profile and parameters.



No.	Item	Condition
1	Heating rate	≤3°C/s
2	Soak zone temperature range	≤4°C/s
3	Soak time	60s~120s
4	Peak temperature	240°C~245°C
5	Time above liquidus (>217°C)	30s~90s
6	Cooling rate	<5°C/s

Figure 17. Typical lead-free reflow soldering profile and parameters.

Note 4: During soldering, the parameters above may be optimized based on the actual component layout. However,the peak temperature must not exceed 245° C. If thick or large metal components require temperatures exceeding 245 °C, thermal shielding measures must be applied to the power module to ensure the actual soldering temperature does not exceed 245°C.

5. Cleaning Clean

using a water-based cleaning agent, followed by drying. Users may adjust the soldering and cleaning processes based on actual conditions, but ultrasonic cleaning is not recommended.

6. Inspection

Inspect the appearance under a microscope to ensure compliance with requirements.

7. X-ray Imaging

Perform X-ray inspection to check solder joint positions, verify solder void compliance, and detect any short circuits. After confirming compliance of the first 1-3 samples, proceed with batch reflow soldering.

Trouble shooting

If a suspected malfunction is observed after device assembly, perform the following checks:
Open Circuit: Inspect solder joints for cold solder joints, insufficient pin soldering, or poor soldering.
No Output: Check the output capacitors near the module.
Short Circuit: Use X-RAY to inspect for internal or external short circuits.

Removal Process

Before removing the product module from the PCB , bake the PCB at 125°C for 48 hours to ensure the module remains unaffected. If baking is omitted, there is a risk of delamination between the plastic module and the substrate. In severe cases, internal solder may melt and flow through delamination gaps, leading to module failure.
For module removal, use a BGA rework station. Handheld hot air guns are not recommended (temperature may exceed 245°C). The product may only be reworked once.

Precautions

The device must be handled with anti-static measures. Wear anti-static gloves when handling the module to prevent electrostatic discharge (ESD) damage caused by human body charges.
Recommended Operational Practices:
a) Operate the device on an anti-static workbench or use finger cots.
b) Ensure all testing equipment and tools are properly grounded.
c) Avoid touching the device leads directly.d) Store the device in anti-static containers (e.g., ESD-safe boxes).
e) During production, testing, usage, and transportation, avoid materials that generate static electricity (e.g., plastics, rubber, silk fabrics).
f) Maintain relative humidity between 30%RH~70% RH.