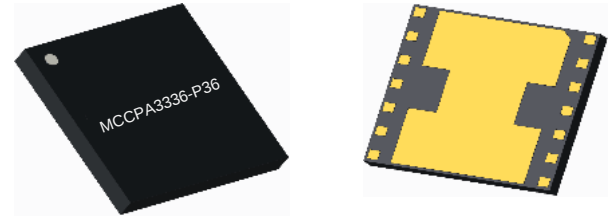


Product Overview

The MCCPA3336-P36 is a three-stage HBT small cell power amplifier for indoor cellular base stations. It works at 3300-3600MHz (B42, n78). This PA can deliver 27dBm 5G output power with ACPR below -47dBc and power gain higher than 30dB.

ROHS compliant

Evaluation boards are available upon request.



14Pin 7×7 mm Laminate Package

Figure1.

Functional Block Diagram

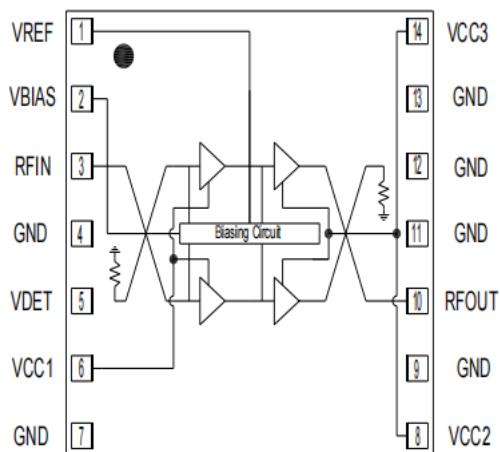


Figure2.

Key Features

- Frequency Range: 3300-3600MHz
- 31dB Gain
- 11% PAE at 27dBm output power
- Below -47dBc ACPR at 27dBm output power w/o DPD with 100M 5G NR signal
- Integrated temperature compensation circuits
- Input/Output internally matched to 50Ω
- On-chip PA enable controller and temperature compensation circuits
- Compact and low-cost 7mm×7mm LGA package (MSL3,260 per JEDEC J-STD-020)

Applications

- FDD and TDD 2G/3G/4G LTE/5G NR systems
- 3GPP band n78 for 5G base stations
- Customer Premises Equipment (CPE)
- Active antenna array and massive MIMO
- Driver amplifier for micro-base and macro-base stations

Ordering info

Part No.	Description
MCCPA3336-P36	7' Reel with 1500pcs

Pin Description

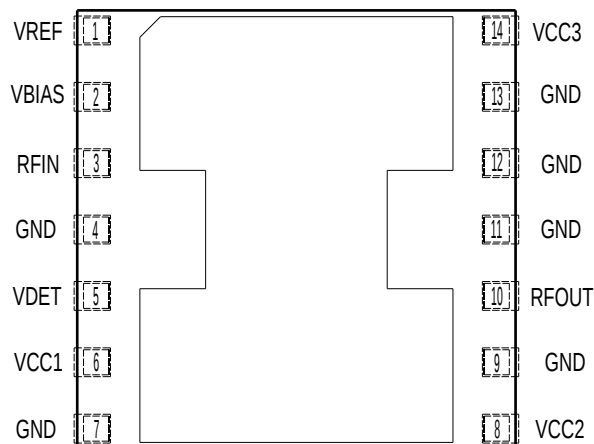


Figure 3. Pinout (Top View)

Pin	Name	Description	Pin	Name	Description
1	VREF	Reference Voltage	8	VCC2	Stage 2 collector voltage
2	VBIAS	Bias Voltage	9	GND	Ground
3	RFIN	RF input port	10	RFOUT	RF output port
4	GND	Ground	11	GND	Ground
5	VDET	Power detector	12	GND	Ground
6	VCC1	Stage 1 collector voltage	13	GND	Ground
7	GND	Ground	14	VCC3	Stage 3 collector voltage

Absolute Maximum Ratings¹

Parameter	Rating	Unit
Operating Temp, T _c	-40 to +85	
Operating Junction Temp, T _j	175	
Storage Temp, T _{STG}	-55 to +125	
Thermal Resistance, R _{θjc}	13.4	/W
Operating Voltage, VCC1, VCC2, VCC3, VBIAS	5.5	V
Input Power, P _{IN}	10	dBm

Notes¹: Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of the Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Voltage VCC1, VCC2, VCC3, VBIAS	4.5	5	5.5	V
Operating Frequency, F	3300		3600	MHz
Operating Temperature, Tc	-40	25	85	
Reference Voltage, VREF	2.6	3.0	3.2	V
Reference Current, IREF		20	30	mA

Electrical Specifications¹

Parameter	Conditions	Min	Typ	Max	Unit
Frequency		3300		3600	MHz
Output average power			27		dBm
Output P3dB	Pulse 10%, 100us		36		dBm
Gain @27dBm			33		dB
Power Added Efficiency			11		%
Quiescent Current			650		mA
ACPR@27dBm	20MHz LTE TM3.1, 9.5dB PAR		-50		dBc
ACPR@27dBm	100M 5G NR, 9.5dB PAR		-47		dBc
Input Return Loss			-15		dB
Output return loss			/		dB
Instantaneous Bandwidth			100		MHZ
Input/Output Impedance			50		Ω

Notes¹: VCC1=VCC2=VCC3=VBIAS=5V, VREF=3.0V F=3500MHz, TC=25 , Input/Output Load=50Ω

Detector Specifications¹

Output Power(dBm)	V _{DET} (mV)	Output Power(dBm)	V _{DET} (mV)
27	617	21	395
26	568	20	372
25	525	19	351
24	486	18	332
23	453	17	317
22	421	RFOff	223

Notes¹: VCC1=VCC2=VBIAS=5V, VREF=3.0V, F=3500MHz, Signal=CW, TC=+25 , Input/Output Load=50Ω

Evaluation Board Schematic

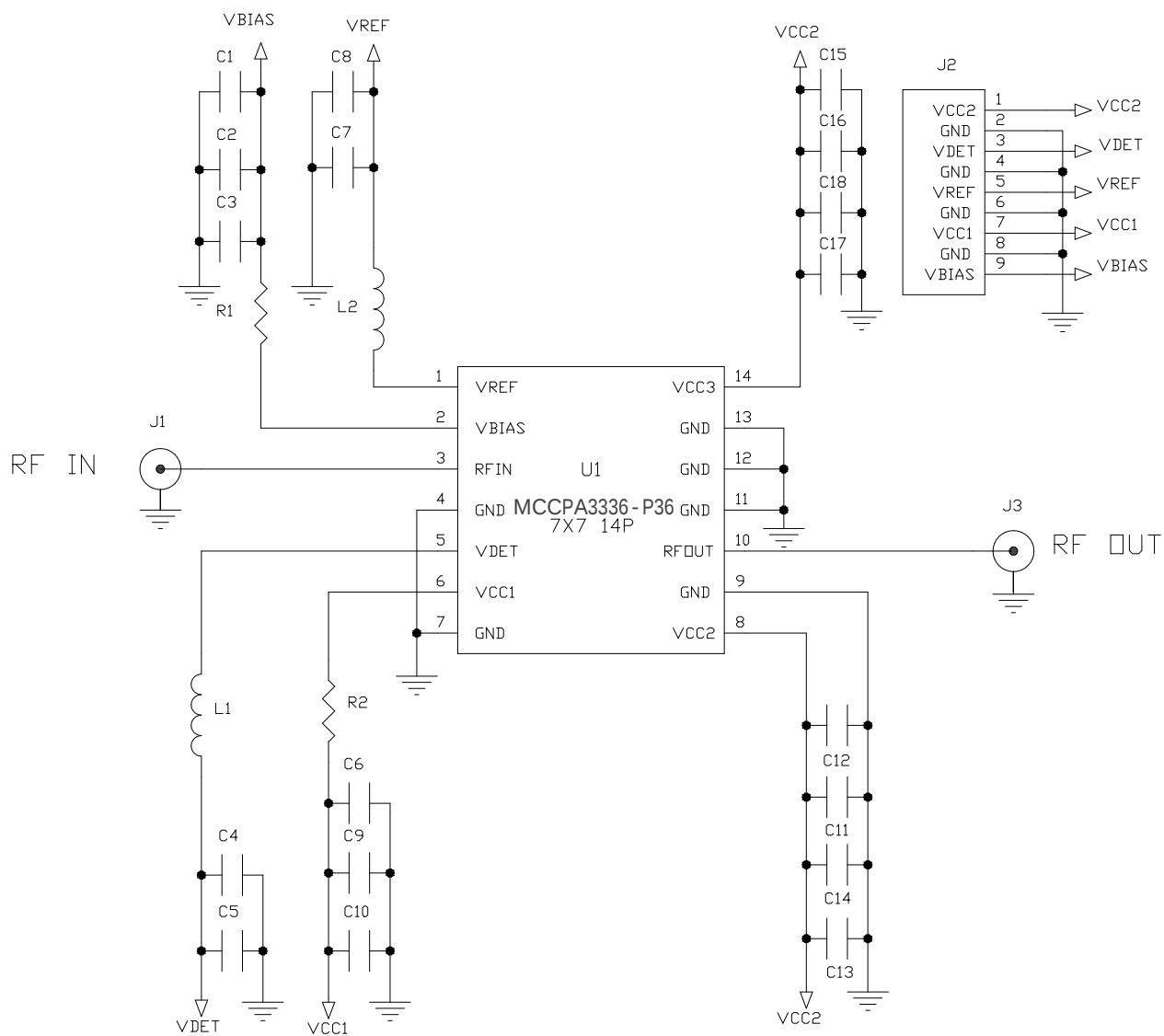


Figure 4. Evaluation Board Schematic

Evaluation Board Bill of Materials

Ref,Des	Value	Size
C1 C14 C15 C8 C10	Ceramic capacitor, 4.7uF, 16V, +/-10%, X7R	1206
L1 L2 R1 R2	Resistor, 0Ω, 0.063W	0402
C4	Ceramic capacitor, 2.2nF, 16V, +/-10%, X7R	0402

Rest of Components on the schematic are not used in this part.

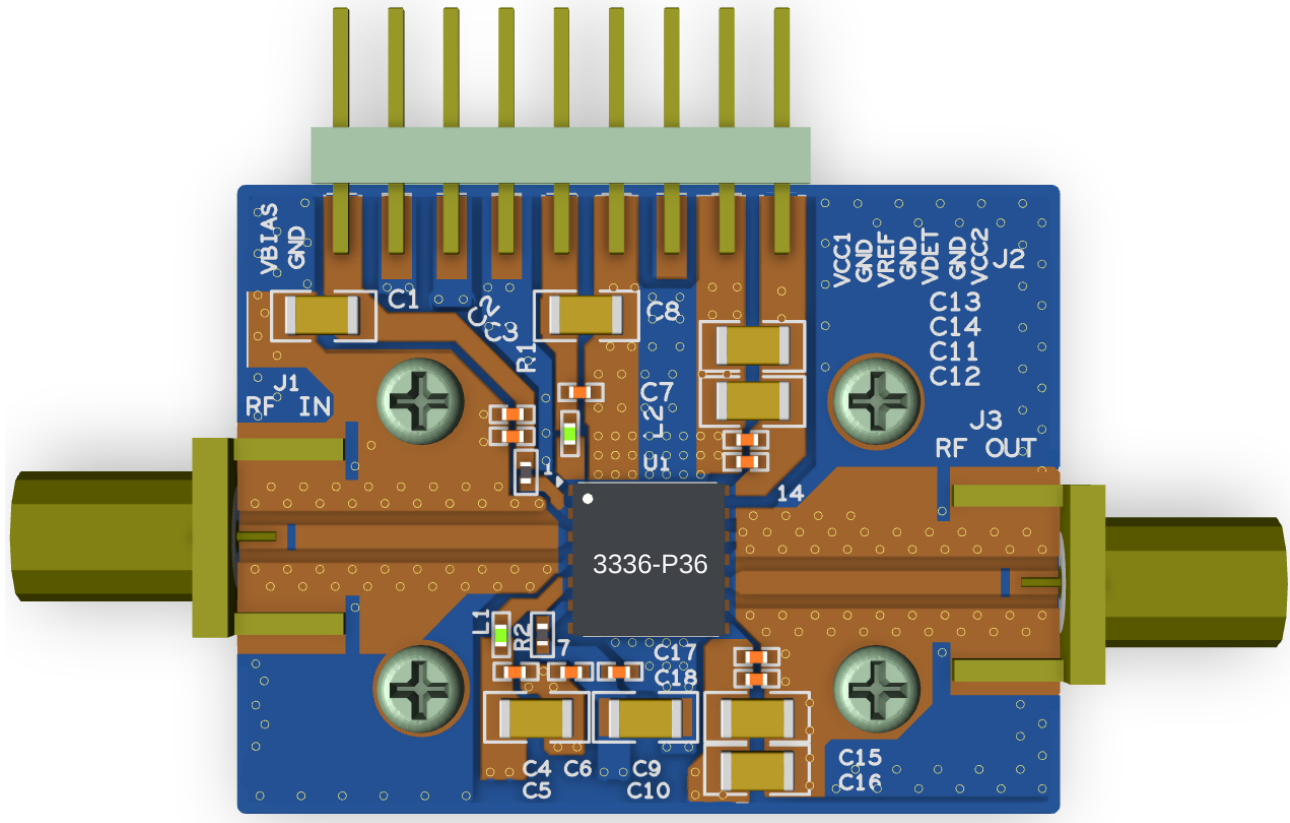


Figure 5 .Evaluation Board PCB information

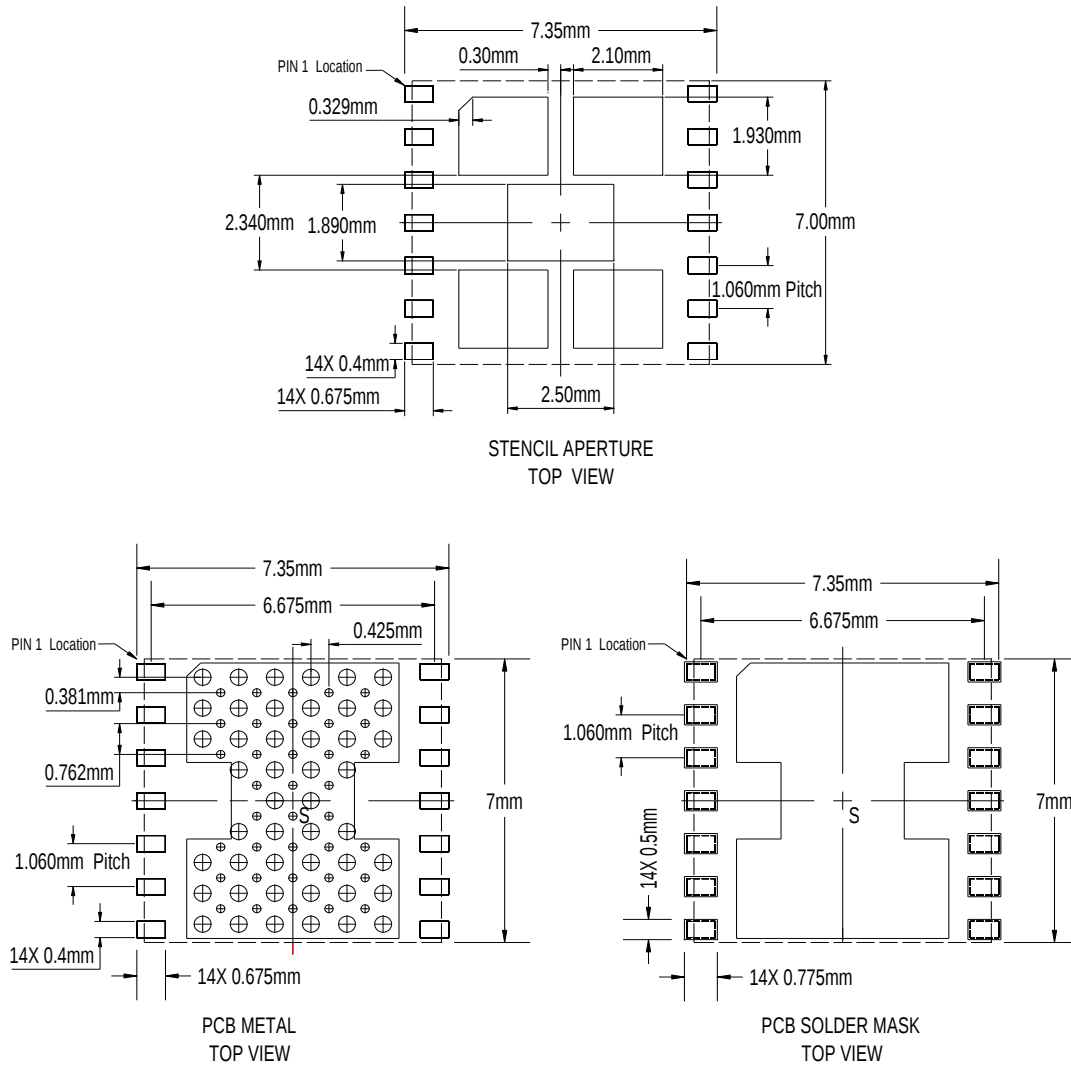
Evaluation Board Test Procedure

Turn-on sequence

- 1.Connect test equipment to the input and output port of Evaluation board and then connect DC ground.
- 2.Turn on VCC1,VCC2,VCC3 to 5V,turn on VBIAS to 5V then turn on VREF to 3.1V in order.
- 3.Apply RF signal

Turn-on sequence

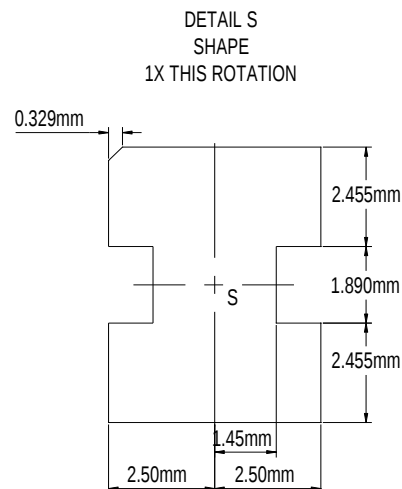
- 1.Turn off RF signal
- 2.Turn off VREF,VBIAS,VCC1,VCC2 and VCC3 in order



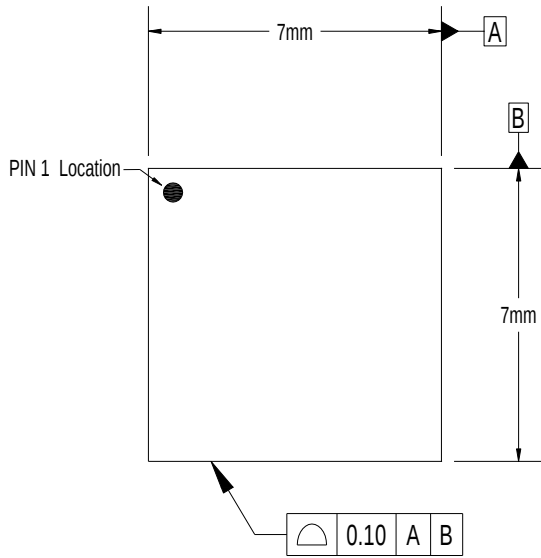
Notes:

1. Unless specified dimensions are symmetrical about center lines shown.
2. Vias shown in PCB metal view are for reference only. Number & Size of thermal vias required dependent on heat dissipation requirement and the pcb process capability.

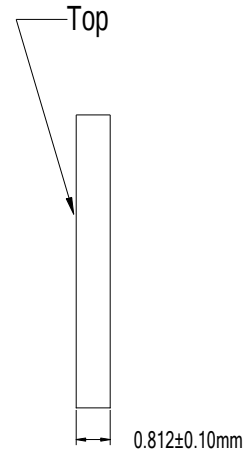
Figure 6. PCB Layout Footprint



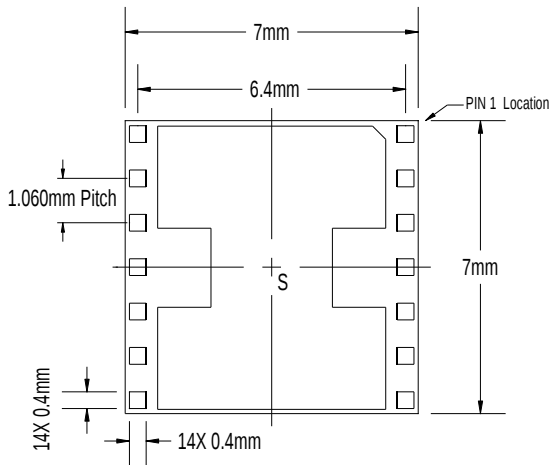
Package Dimensions



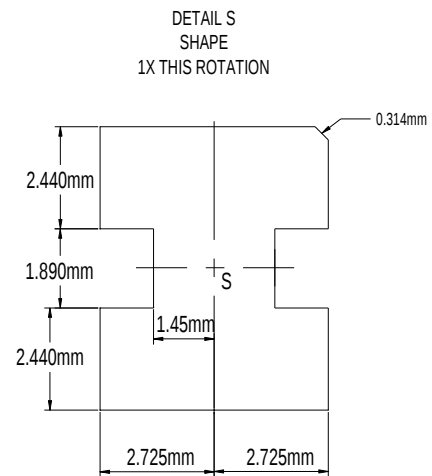
Top View



Side View



Bottom View

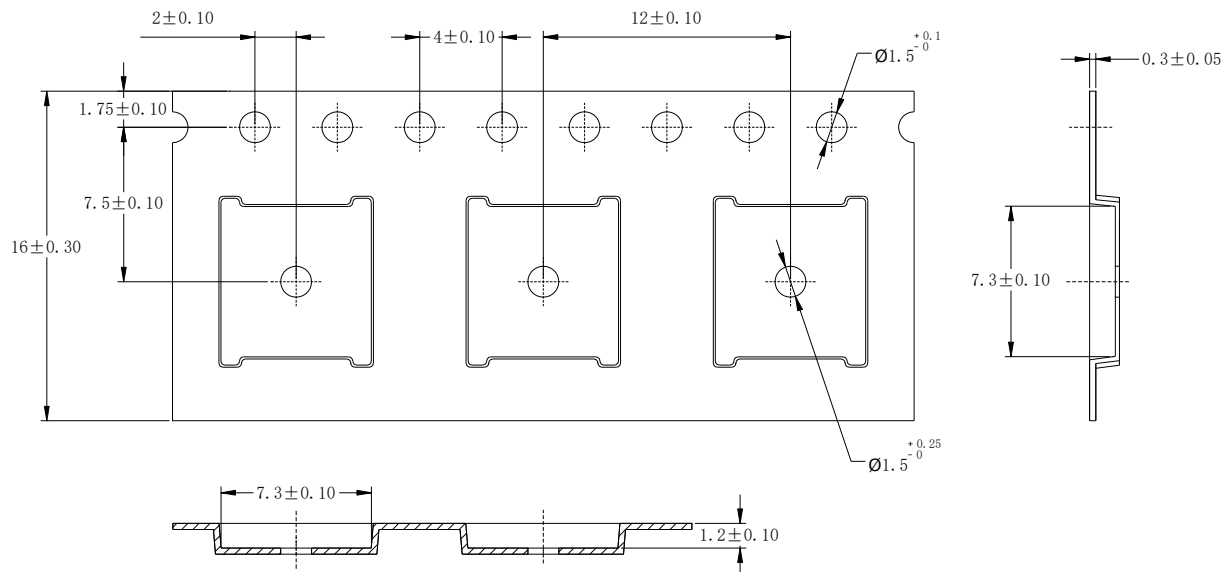


Notes:

1. Tolerance is $\pm 0.050\text{mm}$ unless otherwise specified.
2. Among the 14 pins on both sides, the size of the GND pin is 0.06mm larger than that of the other pins

Figure 7. Package Dimensions

Tape and Reel Information



Technical requirements:

1. Cover tape color: Black
2. The material: PS
3. Mold# BGA/LGA/QFN(7×7)
4. Cover tape width: 13.3 ± 0.1 mm
5. Cover tape color: transparent

Figure 8