MCDCM4644

Quad 4A & Single 16A DC/DC Converter

Features

- Input Voltage Range: 4.0V～14V
- Adjustable Output Voltage: 0.6V～5.5V
- Output Current: Quad 4A or Single 16A
- Voltage Regulation: 0.1% (Typ.)
- Load Regulation: 0.5% (Typ.)
- Multi-phase Parallel Current Sharing
- Current Mode Control, Fast Transient Response
- PGOOD Function
- Built-in Temperature Monitoring Diode
- Selectable CCM and DCM Modes
- Over-Current, Short-Circuit, and Over-Temperature Protection
- Dimensions: 15mm×9mm×5.00mm

Applications

- FPGA/DSP Power Supply
- Multi-Voltage Rail Systems

Description

The MCDCM4644 is a fully integrated quad-channel DC/DC converter with 4A output per channel (or 16A in single-channel mode) and a wide input voltage range. It is available in LGA and BGA packages, integrating the switching controller, power FETs, inductors, an al supporting components.

The input voltage range of the MCDC4644M is 4V to 14V, delivering four independently adjustable output voltages from 0.6V to 5.5V (each set by a single external resistor). External components only require bulk capacitors at the input and output (recommended: ceramic capacitors or a combination).

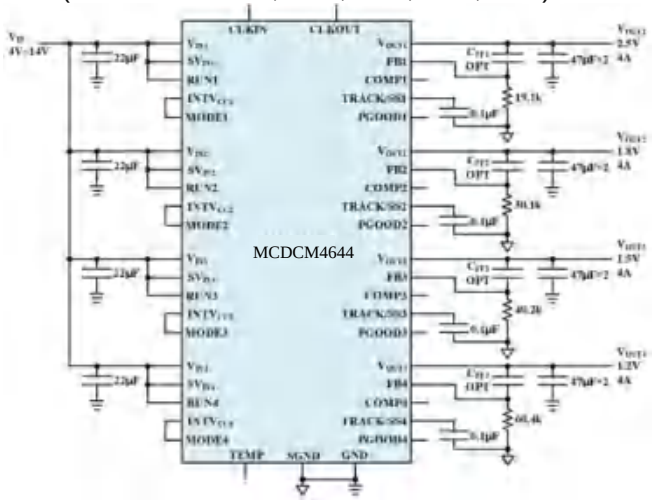
The MCDCM4644 provides stable power supply voltages for digital circuits such as FPGAs and DSPs, supporting continuous output currents of up to 4A per channel. When configured in multi-phase parallel mode, it delivers up to 8A (2-phase) or 16A (4-phase) output current.

As a compact surface-mount module, the MCDCM4644 is assembled onto PCBs using reflow soldering.Its design features small size, high integration, and lightweight construction.

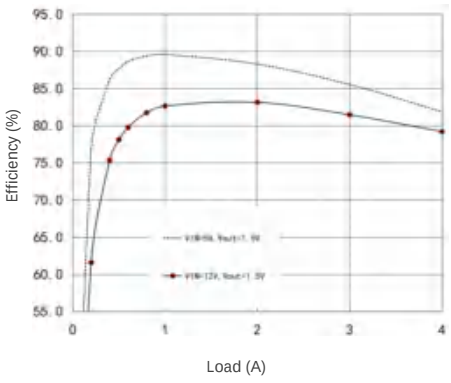
Typical Application

Typical application circuit for the quad independent operation mode

(4A each channel, 2.5V, 1.8V, 1.5V, 1.2V)



1.5V Output Load Efficiency Curve



AbsoluTe Maximum Ratings Note1

V_{IN},S_{VIN} (per channel)..... -0.3V-15V
V_{OUT}(per channel).....-0.3V-6V
RUN(per channel).....-0.3V～S_{VIN}
$INTV_{CC}$.....-0.3V-3.6V
MODE，PGOOD，TRACK/SS，
FB(per channel) ..... -0.3V-$INTV_{CC}$
CLKOUT，CLKIN..... -0.3V-$INTV_{CC}$
Output Current Range
I_{OUT}.....0-5A Single channel operating independently
I_{OUT}.....Nx(0-5A) N:number of parallel channels
Pin Soldering Temperature Resistance..250°C (30s)
Storage Temperature Range(T_{stg})... - 55°C to 125°C

Recommended Operating Conditions

Input Power Voltage
V_{IN}.....4.0V-14V
Output Voltage Range
V_{OUT}.....0.6-5.5V
Output Current Range
I_{OUT}....0-4A (single-channel standalone operation)
I_{OUT}.....Nx(0-4A) N:number of parallel channels
Operating temperature range (T_j)[Note2] ..-40°C-125°C
Recommended PCB Soldering Temperature Profile:
Standard leaded profile (Peak temperature: 210°C -230°C, Time above liquidus: 30s~90s)
Standard lead-free profile (Peak temperature: 240 °C-245°C, Time above liquidus: 30s~90s).

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Extended operation under absolute maximum conditions may affect device reliability and lifespan.
Note 2: MCDCM4644 is tested under pulsed load conditions to ensure Tj=TA.

Thermal Resistance

Model	Package	Dimensions (mm)	Test Board Size (mm)	Junction-to-Ambient θ_{JA}	Junction-to-Substrate $\theta_{JCbottom}$	Junction-to-Top θ_{JCtop}
MCDCM4644	BGA	15×9×5	≥100×100 (4-layer)	10°C/W	2.75°C/W	17°C/W

Test Conditions: The product is welded onto the test board, which measures 100mm × 100mm × 1.6mm in size. The test board consists of four layers and features heavy copper plating on both the surface and inner layers, with a thickness of 1oz (ounce). Given that thermal resistance parameters are highly dependent on the actual application environment, results obtained under varying conditions may differ to some extent. Therefore, this parameter should be considered as a reference only.

Odering Information

Device Specification	Terminal Material	Package Type	Moisture Sensitivity Level	Temperature Range (T_j)	Quality Grade
MCDCM4644	SAC305	77-BGA	3	-40°C-125°C	Industrial Grade

PIN Configuration

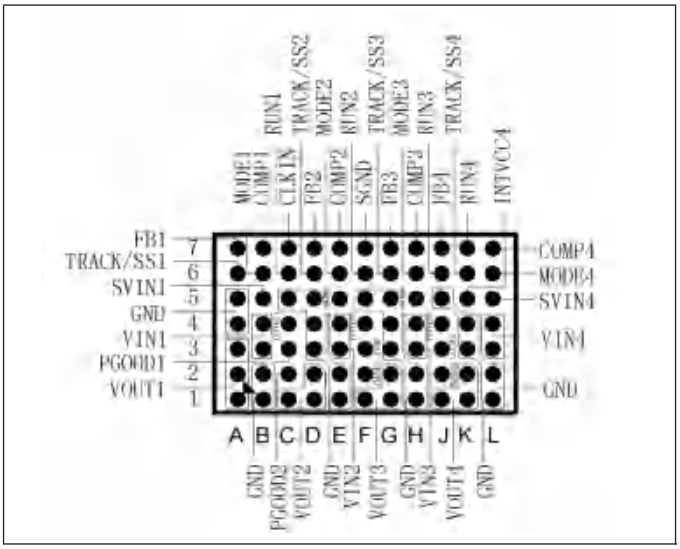


Figure 1. Pin defines the top view

PIN	Definition	Pin Description
B3, B4	V_{IN1}	Power input pins for each channel. It is recommended to place input decoupling capacitors directly between each input and GND.
E3, E4	V_{IN2}	
H3, H4	V_{IN3}	
L3, L4	V_{IN4}	
A1, A2, A3	V_{OUT1}	Power output pins for each channel. Apply the output load between these pins and GND. It is recommended to place output decoupling capacitors directly between each output and GND.
C1, D1, D2	V_{OUT2}	
F1, G1, G2	V_{OUT3}	
J1, K1, K2	V_{OUT4}	
A4-A5, B1-B2, C5, D3-D5, E1-E2, F5, G3-G5, H1-H2, J5, K3-K4, L1-L2	GND	The power ground of each input and output circuit is connected together. A large copper area on the PCB is used to connect all the GNDs.
C3	PGOOD1	Indicator for output status of each channel. PGOOD is pulled to GND if the voltage on the FB pin deviates beyond ±10% of the internal 0.6V reference.
C2	PGOOD2	
F2	PGOOD3	Indicator for output status of each channel. PGOOD is pulled to GND if the voltage on the FB pin deviates beyond ±10% of the internal 0.6V reference. PGOOD is pulled to GND if the voltage on the FB pin deviates beyond ±10% of the internal reference.
J2	PGOOD4	
J3	CLKOUT	Output clock signal for multi-phase operation. CLKOUT is set to 180° phase shift relative to CLKIN. The peak value of CLKOUT ranges from INTVCC to GND.

PIN	Definition	Pin Description
C4	INTVCC1	Internal 3.3V regulator output for each channel. Powers the control circuit and internal gate drivers. Each pin is internally coupled to GND via a 2.2μF low-ESR ceramic capacitor.
F4	INTVCC2	
J5	INTVCC3	
K5	INTVCC4	
C7	CLKIN	External synchronization clock input.
F7	SGND	Signal ground connection. Internally connected to GND at a single point.
F3	TEMP	Internal temperature-sensing diode output. Monitors the VBE junction voltage variation with temperature.
B5	SVIN	
E5	SVIN2	Signal input for each channel. Internally connected to VIN via a low-pass filter to supply the internal 3.3V regulator.
H5	SVIN3	
L5	SVIN4	
A6	TRACK/SS1	Output voltage tracking and soft-start input for each channel. Allows control of the output voltage ramp-up time. Applying a voltage below 0.9V bypasses the internal reference to the error amplifier, ensuring FB pin voltage tracks the TRACK voltage. Tracking stops when this pin voltage exceeds 0.9V
D6	TRACK/SS2	
G6	TRACK/SS3	
K6	TRACK/SS4	
B6	MODE1	Operating mode selection for each channel. Connect to INTVCC to enforce Continuous Conduction Mode (CCM) under all loads. Connect to SGND to enable Discontinuous Conduction Mode (DCM). Do not leave this pin floatingduring normal operation.
E6	MODE2	
H6	MODE3	
L6	MODE4	
C6	RUN1	Operating mode selection for each channel. Connect to INTVCC to enforce Continuous Conduction Mode (CCM) under all loads. Connect to SGND to enable Discontinuous Conduction Mode (DCM). Do not leave this pin floatingduring normal operation.
F6	RUN2	
J6	RUN3	
K7	RUN4	
A7	FB1	Inverting input of the error amplifier for each channel. Internally connected to VOUT via a 60.4kΩ precision resistor. Output voltage can be adjusted by adding an external resistor between FB and GND. For parallel operation, connect all FB pins together.
D7	FB2	
G7	FB3	
J7	FB4	
B7	COMP1	Current control threshold setting and error amplifier compensation for each channel. The current comparator threshold increases with this control voltage . Connect all COMP pins together in parallel operation.
E7	COMP2	
H7	COMP3	
L7	COMP4	

Electrical Characteristics

Symbol	Parameter	Test Condition (Note 3)	Limits			Unit
			Min	Typ	Max	
V_{IN}	Input Voltage Range	$SV_{IN}=V_{IN}$	4.0	–	14.0	V
$V_{OUT(RANGE)}$	Output Voltage Range	—	0.6	–	5.5	V
$V_{OUT(DC)}$	Output Voltage	C_{IN}=22μF，C_{OUT}=47μF×2，MODE=$INTV_{CC}$，V_{IN}=4.0V~14V，R_{FB}=40.2kΩ，I_{OUT}=0~4A (Note4)	1.460	1.5	1.540	V
Input Characteristic						
$V_{IN(UVLO)}$	Input Undervoltage Threshold	V_{IN} falling	2.4	2.6	2.8	V
		V_{IN} hysteresis	—	350	—	mV
$I_{Q(SVIN)}$	Quiescent Current	V_{IN}=12V，V_{OUT}=1.5V，MODE=$INTV_{CC}$	—	8	—	mA
		V_{IN}=12V，V_{OUT}=1.5V，MODE=GND	—	2	—	mA
		Shutdown，RUN=0，V_{IN}=12V	—	11	—	μA
$I_{S(VIN)}$	Input Supply Current	V_{IN}=12V，V_{OUT}=1.5V，I_{OUT}=4A	—	0.64	—	A
Output Characteristics						
$I_{OUT(DC)}$	Output Current	V_{IN}=12V，V_{OUT}=1.5V (Note4)	0	—	4	A
S_V	Line Regulation	V_{OUT}=1.5V，I_{OUT}=0A，V_{IN}=4V~14V	—	0.1	1.5	%
S_I	Load Regulation	V_{IN}=12V，V_{OUT}=1.5V，I_{LOAD}=0A~4A	—	0.5	1.5	%
V_{PP}	Output Ripple Voltage	I_{OUT}=2A，C_{OUT}=47μF×2，V_{IN}=12V，V_{OUT}=1.5V	—	10	—	mV
f_{OSC}	Switching Frequency	—	—	1	—	MHz
$\triangle V_{OUT(START)}$	Startup Overshoot	C_{OUT}=47μF×2，V_{IN}=12V，V_{OUT}=1.5V，I_{OUT}=0A	—	35	—	mV
t_{START}	Startup Time	C_{OUT}=47μF×2，no load，TRASK/SS=0.01μF，V_{IN}=12V，V_{OUT}=1.5V	—	2.5	—	ms
$\triangle V_{OUTLS}$	Dynamic Step Overshoot	Load：0%~50%~0%，C_{OUT}≥47μF，V_{IN}=12V，V_{OUT}=1.5V	—	160	—	mV
t_{SETTLE}	Dynamic Recovery Time	Load：0%~50%~0%，C_{OUT}≥47μF，V_{IN}=12V，V_{OUT}=1.5V	—	45	—	μs
I_{OUTPK}	Output Current Limit	V_{IN}=12V，V_{OUT}=1.5V	5	6	—	A
Control Section						
V_{FB}	FB Pin Voltage	V_{IN}=12V，V_{OUT}=1.5V，I_{OUT}=0A	0.591	0.600	0.609	V
V_{RUN}	RUN Enable Threshold	V_{RUN} rising edge	1.0	1.2	1.4	V
V_{PGOOD}	PGOOD Trip Level	V_{FB} ramp-up (negative)	-13	-10	-7	%
		V_{FB} ramp-up (positive)	7	10	13	%

Note 3: Electrical parameter testing results are based on the module soldered onto the evaluation board.

Note 4: Refer to the output current derating curves for different V_{IN}, V_{OUT}, and T_A conditions.

Product Principle Block Diagram

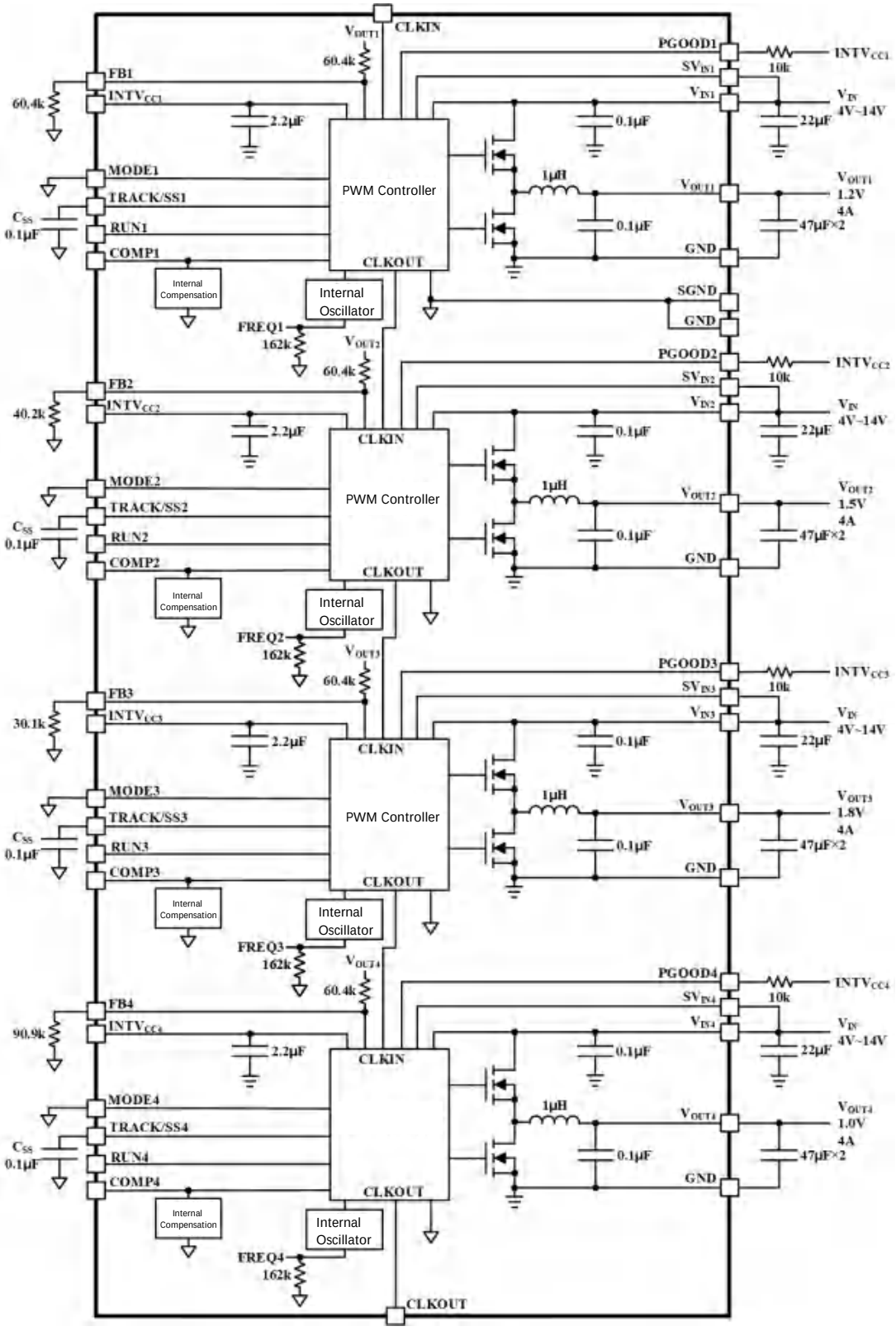


Figure 2 Block diagram of the principle of MCDCM4644

Typical Performance Characteristics

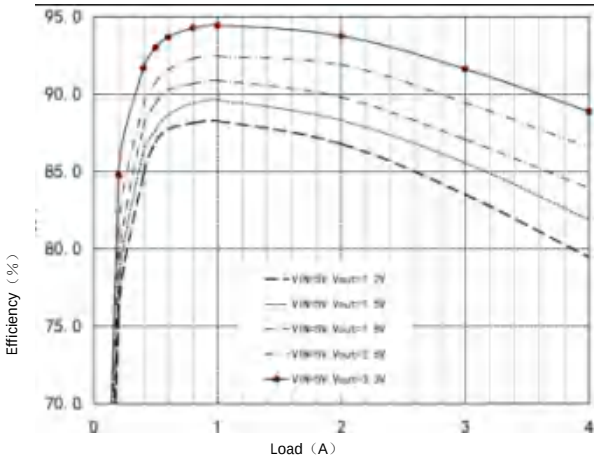


Figure 3 5V input-load-efficiency curve

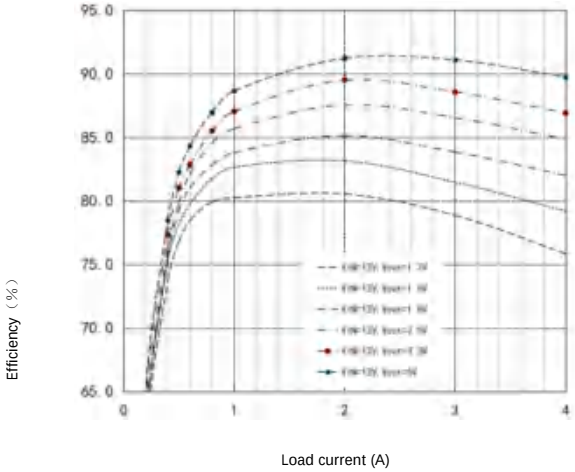
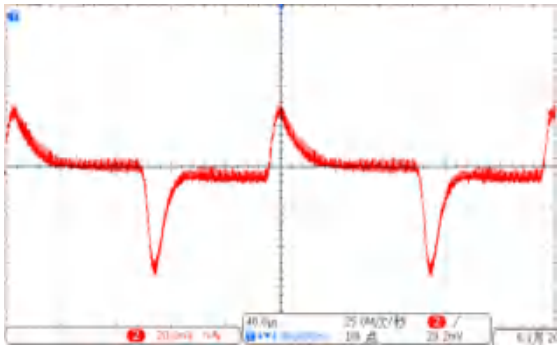


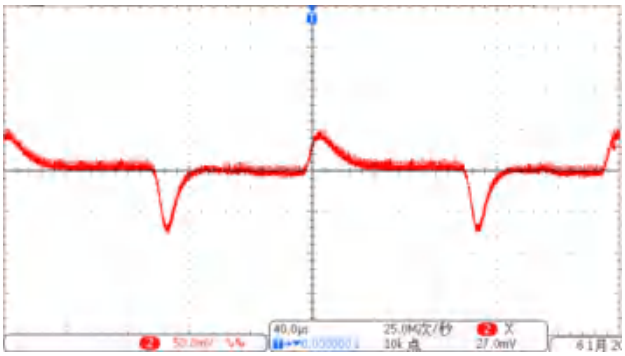
Figure 4 12V input-load-efficiency curve



V_{IN}=12V；V_{OUT}=1.0V；I_{OUT}=0~2A~0；

f=5kHz, C_{OUT}=47μF(ceramic)×2

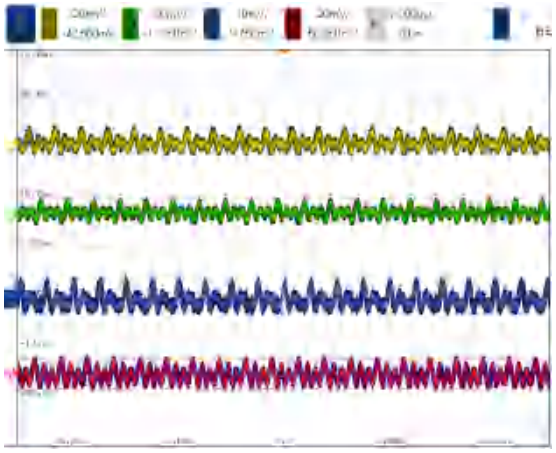
Figure 5 Load-dynamic curve



V_{IN}=12V；V_{OUT}=1.5V；I_{OUT}=0~2A~0；

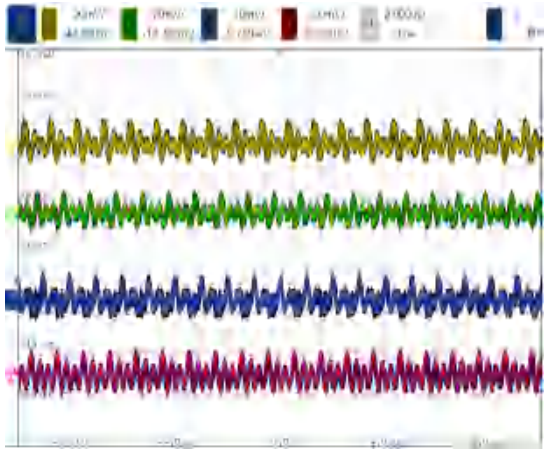
f=5kHz, C_{OUT}=47μF(ceramic)×2

Figure 6 Load-dynamic curve



V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=2A,
BW：20MHz, C_{OUT}=47μF(ceramic)×2

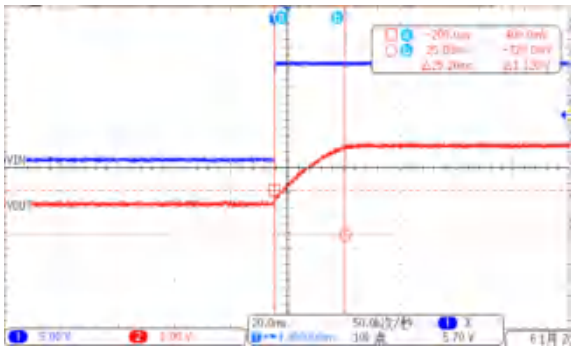
Figure 7. Output Ripple Voltage



V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=2A,
BW：20MHz, C_{OUT}=47μF(ceramic)×2

Figure 8. Output Ripple Voltage

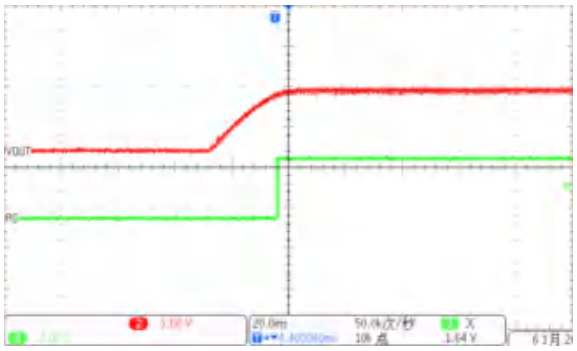
Typical Performance Characteristics



V_{IN}=12V，V_{OUT}=1.5V，I_{OUT}=0A，

C_{OUT}=47μF (ceramic)x2，C_{SS}=0.1μF

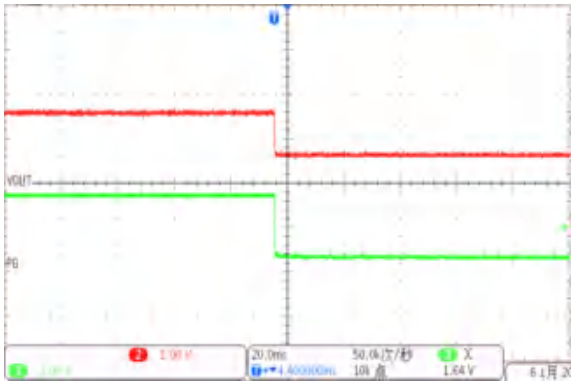
Figure 9. Startup Waveform - No Load



V_{IN}=12V，V_{OUT}=1.5V，V_{PGOOD}=3.3V，I_{OUT}=2A

C_{OUT}=47μF(ceramic)×2，C_{SS}=0.1μF

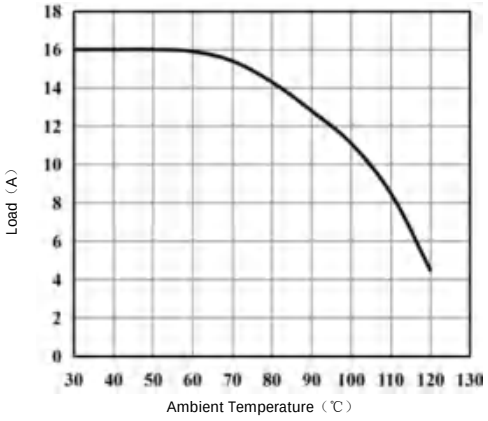
Figure 10. Startup Waveform - 2A Load



V_{IN}=12V，V_{OUT}=1.5V，V_{PGOOD}=3.3V，I_{OUT}=2A

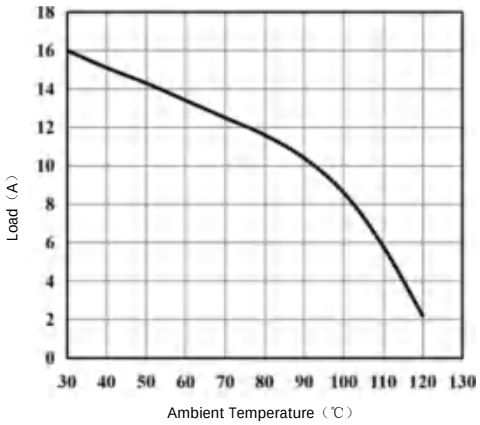
C_{OUT}=47μF (ceramic)×2，C_{SS}=0.1μF

Figure 11. Discharge Waveform - 2A Load



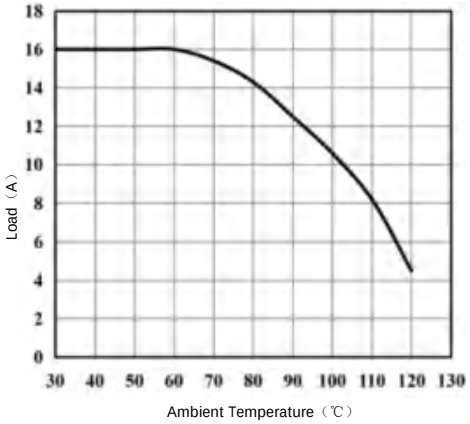
V_{IN}=5V，V_{OUT}=1.0V，
Four-way parallel connection

Figure 12. Reduction Curve



V_{IN}=12V，V_{OUT}=1.0V，
Four-way parallel connection

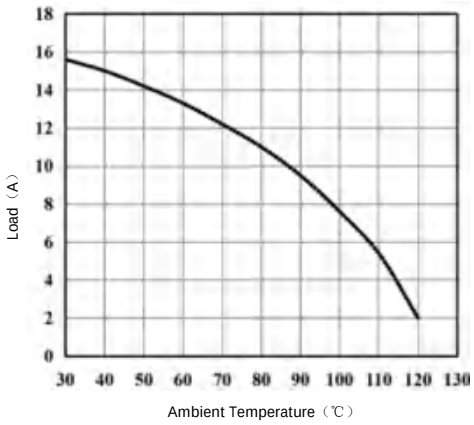
Figure 13. Downgrading Curve



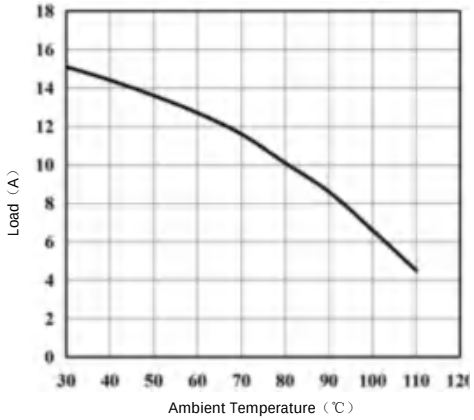
V_{IN}=5V，V_{OUT}=1.5V，
Four-way parallel connection

Figure 14. Downgrading Curve

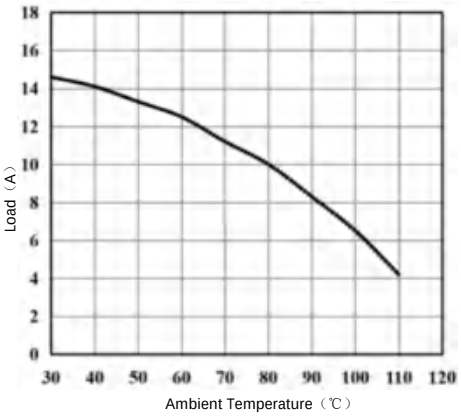
Typical Performance Characteristics



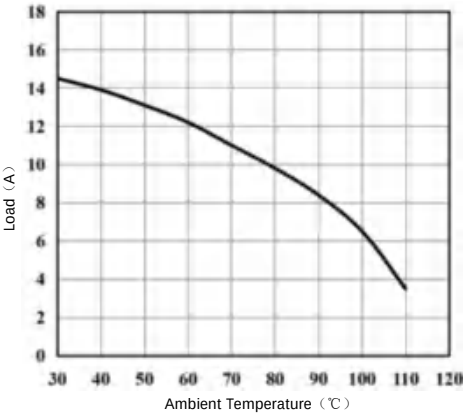
V_{IN}=12V，V_{OUT}=1.5V，
Four-way parallel connection
Figure 15. Downgrading Curve



V_{IN}=5V，V_{OUT}=3.3V
Four-way parallel connection
Figure 16. Downgrading Curve



V_{IN}=12V，V_{OUT}=3.3V，
Four-way parallel connection
Figure 17. Downgrading Curve



V_{IN}=12V，V_{OUT}=3.3V，
Four-way parallel connection
Figure 18. Downgrading Curve

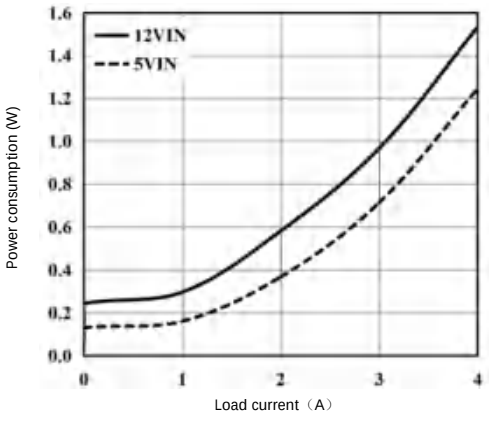


Figure 19. Power consumption curve at 1.2V output voltage (single channel, 25℃)

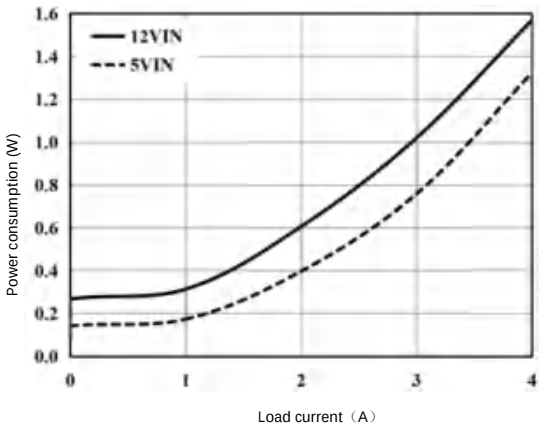


Figure 20. Power consumption curve at 1.5V output voltage (single channel, 25℃)

Typical Performance Characteristics

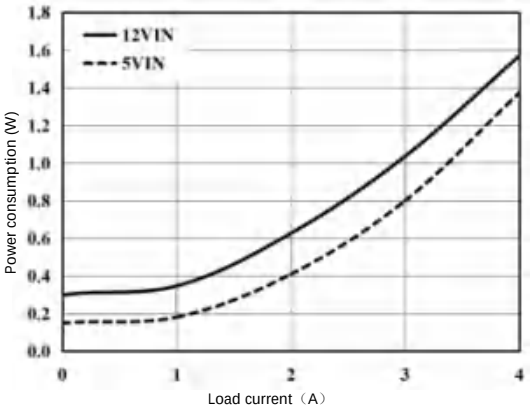


Figure 21. Power consumption curve at 1.8V output voltage (single channel, 25℃)

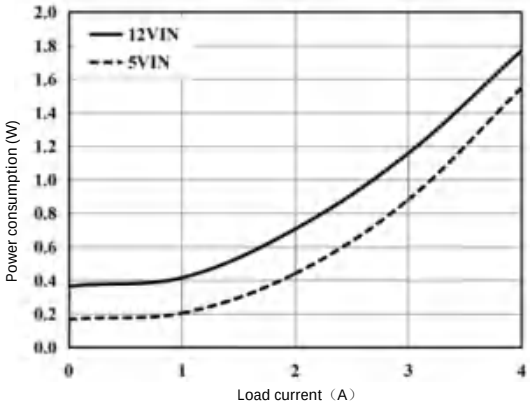


Figure 22. Power consumption curve at 2.5V output voltage (single channel, 25)

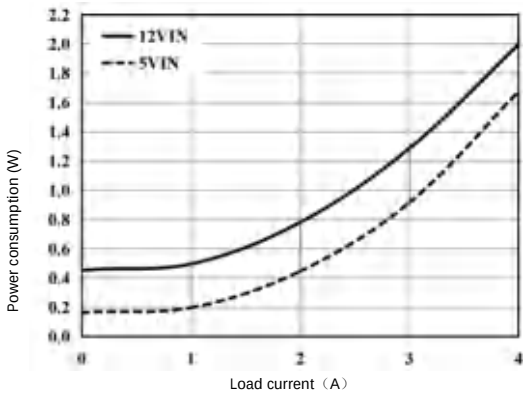


Figure 23. Power consumption curve at 3.3V output voltage (single channel, 25℃)

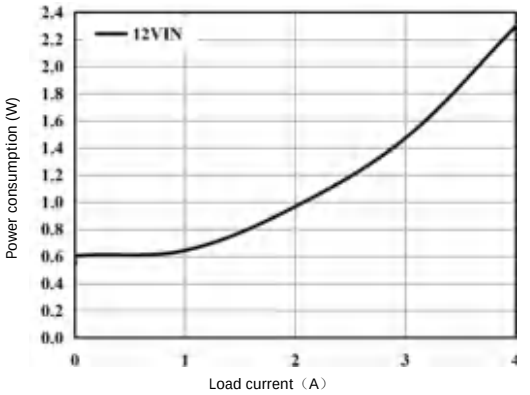


Figure 24. Power consumption curve at 5.0V output voltage (single channel, 25℃)

V_{IN} to V_{OUT} Step-Down Converter

The maximum duty cycle of each channel is limited by the minimum off-time, and the minimum duty cycle is limited by the minimum on-time.

The minimum off-time restricts the maximum duty cycle. To prevent excessive voltage drop under heavy loads, the maximum duty cycle is generally recommended not to exceed 75%. It can be calculated as:

$$D_{MAX} = 1 - t_{OFF(MIN)} \times f_{SW}$$

Here, $t_{OFF(MIN)}$ represent the minimum off-time (for MCDCM4644, the typical valueis 70ns), and f_{SW} is the switching frequency. Conversely, the minimum on-time limits the minimum duty cycle, calculated as:

$$D_{MIN} = t_{ON(MIN)} \times f_{SW}$$

Here, $t_{ON(MIN)}$ denote the minimum on-time (for MCDCM4644, the typical valueis 20ns). If the actual duty cycle falls below the minimum, the output voltage remains adjustable, but the switching frequency decreases. Refer to Figure 12-18 in the product manual for the frequency derating curve under standard design conditions.

Output Voltage

The PWM controller's reference voltage is 0.6V. As shown in the schematic, a 60.4kΩ high-frequency feedback resistor is connected between the V_{OUT} pin and FB pin of each regulator. A resistor R_{FB} added between the FB pin and GND sets the output voltage:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \times 60.4k$$

Table 1: Output Voltage vs. R_{FB} Resistance Values

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB} (kΩ)	Open	90.9	60.4	40.2	30.1	19.1	13.3	8.25

For parallel operation of N channels:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \times \frac{60.4k}{N}$$

Input Decoupling Capacitor

The MCDCM4644 must be connected to a low AC-impedance DC power source. For each regulator channel, a 22μF ceramic input capacitor is recommended for RMS ripple current decoupling. If the input trace is long or the source capacitance is insufficient, a bulk capacitor (either single or fixed) should be added. Ignoring inductor current effects, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \times \sqrt{D \times (1 - D)}$$

Here, η% represents the power module's design efficiency.

Output Decoupling Capacitor

With high-frequency, high-bandwidth design, each regulator channel requires only two 47μF ceramic output capacitors to achieve low output voltage ripple and excellent transient response. To ensure filtering performance and stability, the output filter capacitance per channel should not be less than 47μF. Additional capacitors (e.g., 1μF, 0.1μF, 1000pF) can be added for enhanced high-frequency noise suppression.

Output filter capacitors must be properly connected to the output power loop (refer to the PCB layout diagram). Multiple vias should be used in the layout for multilayer power plane interconnections.

Discontinuous Conduction Mode (DCM)

For light-load conditions requiring high conversion efficiency, Discontinuous Conduction Mode (DCM) is recommended. Connect the MODE pin to SGND to enable DCM. Under light load conditions, the internal current comparator may experience several cycles of fluctuation, thereby forcing the switching transistor MOSFET to remain in the off state for multiple cycles and consequently skipping those cycles. In this mode, the current in the inductor does not reverse direction.

Forced Continuous Conduction Mode

For applications requiring fixed-frequency operation and minimal output ripple, Forced Continuous Conduction Mode (FCCM) should be used. Enable FCCM by connecting the MODE pin to $INTV_{CC}$. In this mode, reverse inductor current is permitted, and the COMP voltage is controlled by a stronger load current threshold. The MOSFET switches on every oscillator pulse cycle.

Switching Frequency

The MCDCM4644's default switching frequency is internally set to 1MHz, optimized for small package size, low output voltage ripple, and high efficiency. Most applications require no additional frequency adjustment. If a frequency other than 1MHz is needed, the module can be synchronized externally to a clock between 700kHz and 1.3MHz.

Frequency Synchronization and Clock Input

The power module includes a Phase-Locked Loop (PLL) consisting of an internal voltage-controlled oscillator and a phase filter. This allows synchronization of all internal MOSFET switching to the rising edge of an external clock. The external clock frequency must be within ±50% of the 1MHz default frequency. A pulse detection circuit monitors the CLKIN pin to activate the PLL. The clock pulse width must be ≥400ns, with a high level >2V and low level <0.3V.

Multi-Channel Parallel Operation

For loads requiring >4A output current, multiple MCDCM4644 regulators can be paralleled to increase output current without raising input/ output voltage ripple. The MCDCM4644 featuresbuilt -in phase shifts between every two of its four regulator channels, supporting configurations suchas 2+2, 3+1, or 4-phase parallel operation. Table 2 presents the phase differences between the stabilizer channels.

Table 2. Phase Difference Between Stabilizer Channels

Channel	CH1	CH2	CH3	CH4
Phase		180℃	90℃	180℃

Figure 25 illustrates the clock phasing schematic for 2+2 and 4-channel parallel configurations.

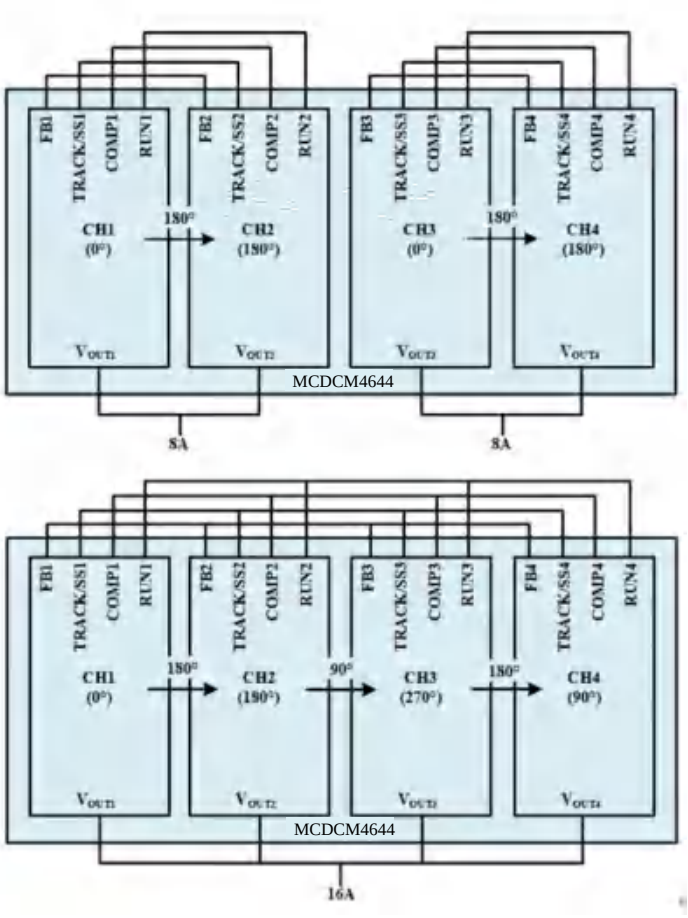


Figure 25. Schematic diagram of the 2+2 and 4-channel parallel connection principle

Multi-phase parallel operation significantly reduces input/output capacitor ripple current. When outputs are combined for high-current designs, the output ripple amplitude decreases proportionally with the phase shift.

The MCDCM4644 device is a current-mode controlled device. Consequently, it exhibits exceptionally favorable current-sharing characteristics when employed in parallel configurations. This feature contributes to heat balancing across the channels.When configuring the device for parallel operation,ensure that the RUN, TRACK/SS, FB, and COMP pins of each parallel channel are connected together.

State-Distributed Output Voltage Tracking

The TRACK/SS pin enables soft-start functionality and synchronized output voltage tracking. Connecting the TRACK/SS pin to the circuit allows configuration of the output voltage control timing. An internal 2.5μA current source charges the external soft-start capacitor to near the INTVcc voltage. When the TRACK/SS voltage is below 0.9V, it overrides the internal 0.6V reference to regulate the output voltage . The total soft-start time is calculated as:

$$t_{SS} = 0.6 \times \frac{C_{SS}}{2.5\,\mu A}$$

where C_{SS} is the capacitance on the TRACK/SS pin.

By configuring the TRACK/SS connection, the output can track the rise or fall of another regulator. Figures 26 and 27 show example waveforms and schematics for proportional tracking, where the slave regulator's output slope (e.g., V_{OUT_S1},V_{OUT_S2},V_{OUT_S3}) is proportional to the master regulator's output (V_{OUT_M})

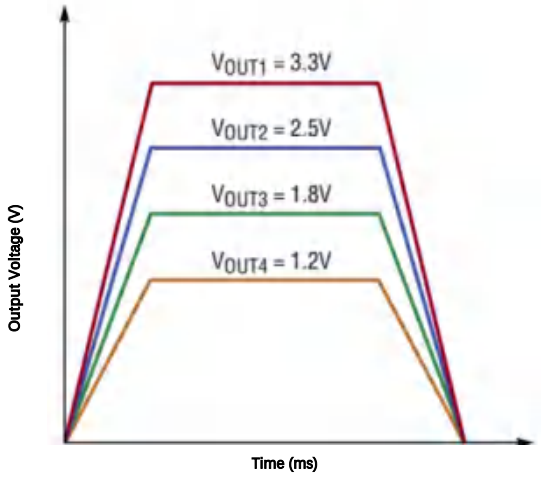


Figure 26. Proportional Output Tracking Waveform

Since the TRACK/SS pin of the slave regulator is connected to the output of the master regulator via an $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider, and the voltage at the TRACK/SS pin (when below 0.9V) is used to regulate the slave regulator's output, the output voltages of the slave and master regulators during startup must satisfy the following equation:

$$V_{OUT(SL)} \times \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \times \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}$$

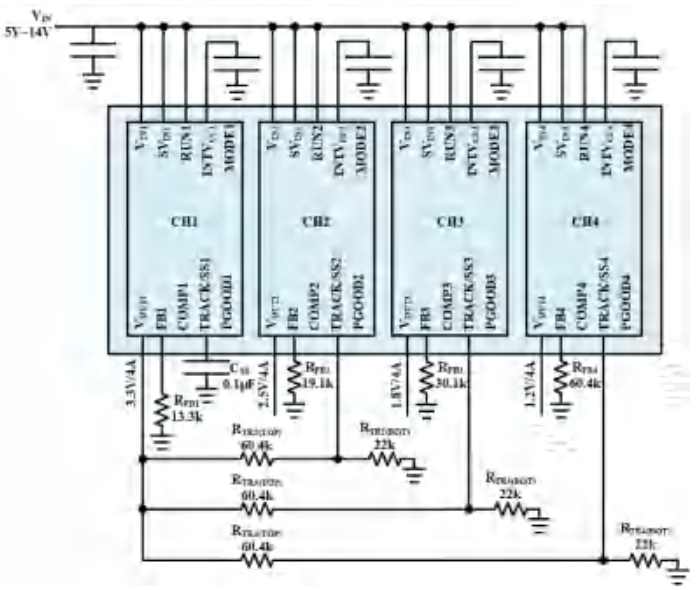


Figure 27. Output Tracking Circuit Diagram

$R_{FB(SL)}$ is the feedback resistor, and $R_{TR(TOP)}/R_{TR(BOT)}$ represents the resistor divider on the TRACK/SS pin of the slave regulator, as shown in Figure 27. According to the formula above, the master regulator's output slope (MR) and the slave regulator's output slope (SR), in units of output voltage/time, are determined by:

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}}$$

Coincident tracking is a special case of proportional tracking where the master and slave output slopes are identical, as shown in Figure 28.

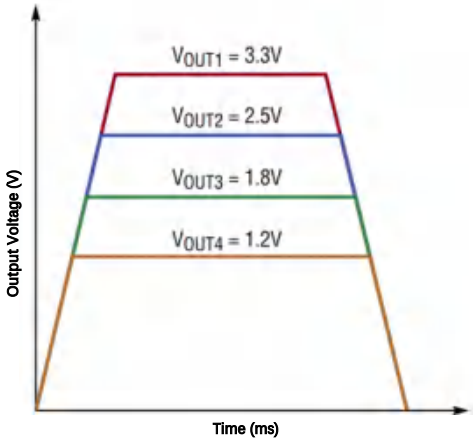
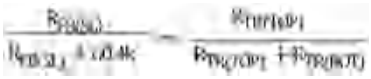


Figure 28. Overlapping Tracking Schematic Diagram

From this equation, it can be observed that in the overlapping tracking process, the resistor divider of the subordinate voltage regulator's TRACK/SS pin is always the same as that of its output divider.



PGOOD Function

The PGOOD pin is an open-drain output indicating whether the output voltage is within ± 10% of its set value. This pin cannot drive high and requires an external pull-up resistor (recommended: 4.7kΩ to 100kΩ), typically connected to the respective channel's $INTV_{CC}$ pin.

Stability Compensation

The internal compensation loop of each regulator is optimized for applications using low-ESR ceramic output capacitors. For scenarios requiring bulk output capacitors or improved transient response, a 10pF to 100pF capacitor (C_{FF}) between V_{OUT} and FB pins enhances phase margin.

Enable Function

The RUN pin serves the function of enabling operation. Specifically, it is utilized to control the activation of the switching-mode DC/DC converter for each channel in the MCDCM4644. When the enable pin is pulled low, the MCDCM4644 enters a shutdown state. If the voltage on the enable pin is below 0.7V, the power transistor remains off.

To turn on the power transistor and allow it to operate, a voltage exceeding 1.2V must be applied to the enable pin.

Over-Temperature Protection

An internal protection circuit monitors the junction temperature of the load monitoring module. If the junction temperature reaches approximately 160° C, both power switches are disabled until the temperature drops by about 25°C.

Low-Input Voltage Applications

The MCDCM4644 module features a dedicated SV_{IN} pin for each regulator channel, enabling operation at input voltages as low as 2.375V. The SV_{IN} pin serves as the power input for the internal control circuitry, while the Vis pin is directly connected to the MOSFET switch terminal. For input voltages ranging from 4V to 14V, the SV_{IN} pin can be directly connected to the V_{IN} pin of each regulator channel. An optional filter (composed of a 10Ω to 100Ω resistor) between SV_{IN} and V_{IN} may be added for enhanced noise immunity, though it is unnecessary in well-designed PCB layouts. For low-input voltage applications (2.375V to 4V) or to reduce power dissipation in the internal isolation LED, SV_{IN} can be connected to an external voltage above 4V via a 0.1μF local bypass capacitor (see Figure 3). Note that the SV_{IN} voltage must not fall below the V_{OUT} voltage.

Temperature Sensing Function

The MCDCM4644 integrates a diode-connected PNP transistor for temperature monitoring via the TEMP pin. By applying a forward current of approximately 100μA through a pull-up resistor , the forward voltage of the diode varies with temperature (see Figure 29 for the temperature-voltage curve).

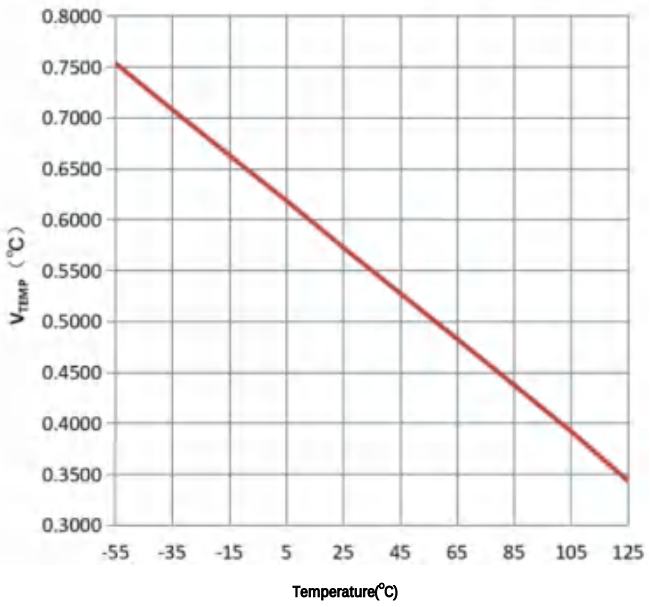


Figure 29. Curve of Forward Voltage of Temperature-Controlled Diode as a Function of Temperature

Recommended PCB Layout

1.Pad Design

It is recommended that the open solder mask windows for large-area copper-coated power pins (e.g., V_{IN}, GND, V_{OUT}, etc.) be adjusted and redesigned. Otherwise, the PCB manufacturing company may apply the default solder mask opening width of approximately 0.1 mm as defined by standard software. This could result in actual solder pads being slightly larger than intended, potentially causing discrepancies between the sizes of the solder pads and independent pins. Inconsistent solder mask windows may lead to the module experiencing solder tension-induced stress in the vertical direction perpendicular to the PCB during reflow soldering, which can cause compression or stretching of solder on other independent pads.

2. PCB Layout

To optimize the electrical and thermal performance of the PCB layout, the following considerations should be implemented:

a. Use large PCB copper areas for high-current paths (e.g., V_{IN}, GND, V_{OUT}) to minimize conduction losses and thermal stress;

b. Place high-frequency ceramic capacitors near the V_{IN}, GND, and V_{OUT} pins to suppress high-frequency noise;

c. Implement a dedicated power ground plane beneath the module;

d. Use multiple vias to connect the top layer with other power layers, minimizing via conduction losses and reducing thermal stress;

e. Avoid placing vias directly on pads unless via-in-pad with filled vias is implemented;

f. For parallel modules, connect the COMP, V_{FB}, RUN, and TRACK/SS pins together. Use an internal layer to interconnect these pins.

Figure 30 provides a recommended PCB layout reference.

3. Recommended Solder Pad

For the MCDCM4644 BGA package, the typical solder ball diameter is 0.76mm. The recommended solder mask opening size for BGA pads in the library is 0.63mm.

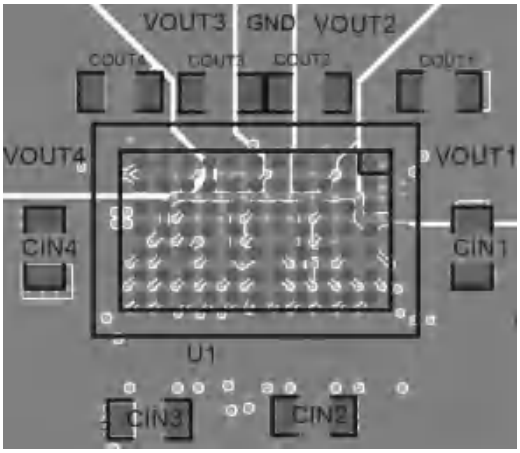


Figure 30. Recommended PCB Board Layout for MCDCM4644

Typical application diagram(Note5)

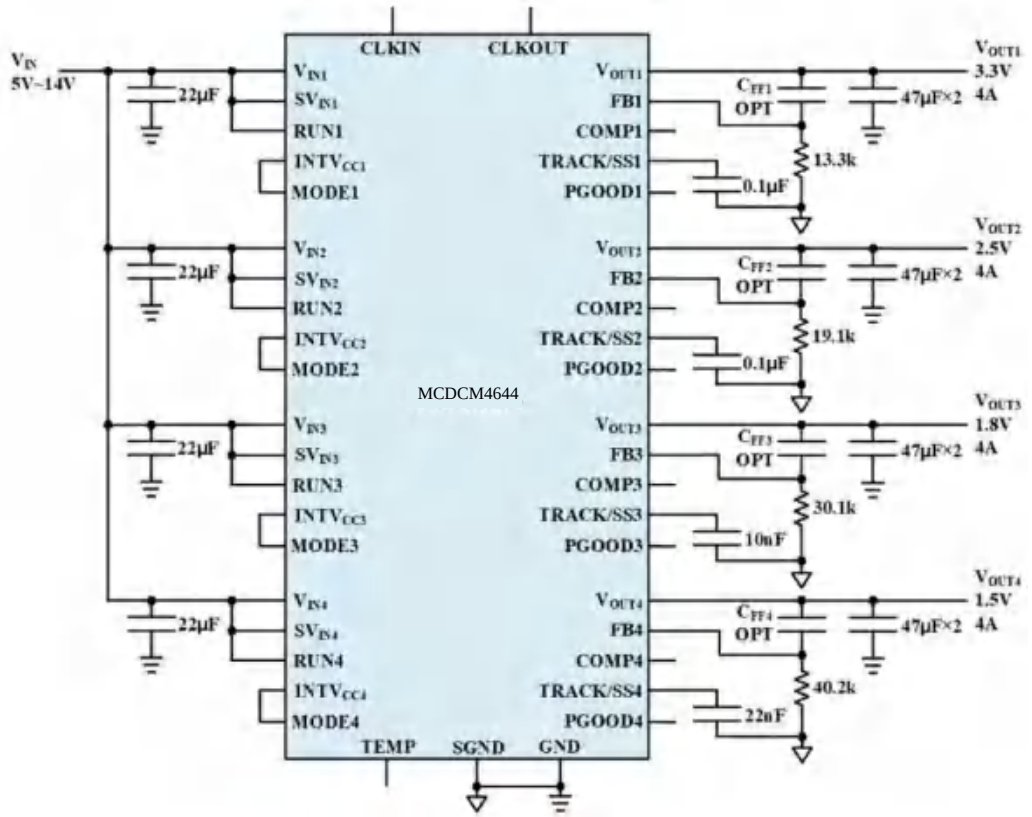


Figure 31. Single path with separate outputs of 3.3V, 2.5V, 1.8V, 1.5V, with a load of 4A

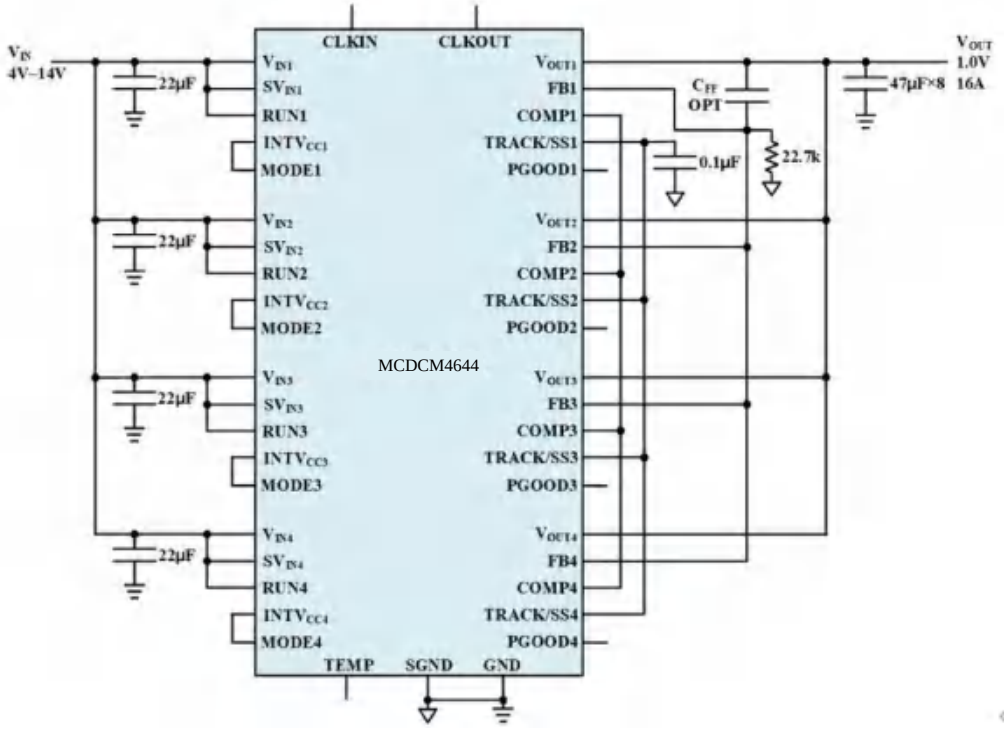


Figure 32. Four-way parallel output of 1.0V, with a load of 16A

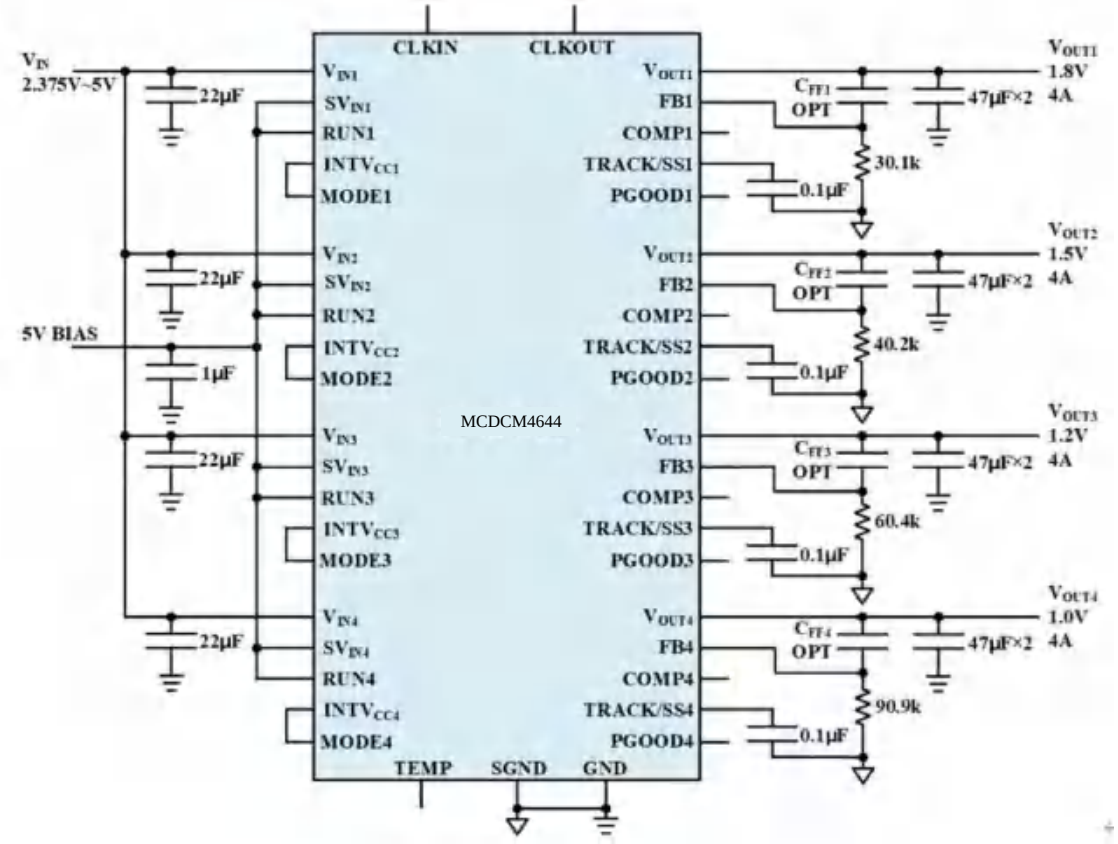


Figure 33. 2.375V to 5V input, 1.8V, 1.5V, 1.2V, 1.0V, load 4A

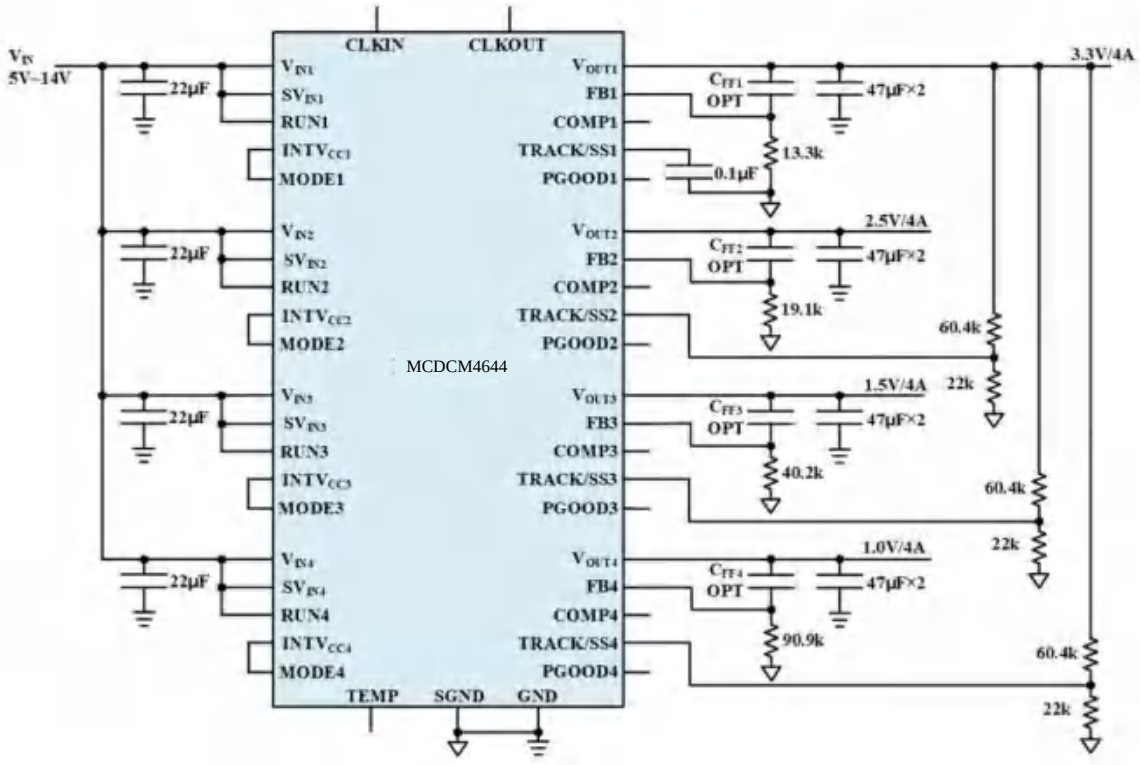


Figure 34. Output Voltage Tracking Mode, Load 4A

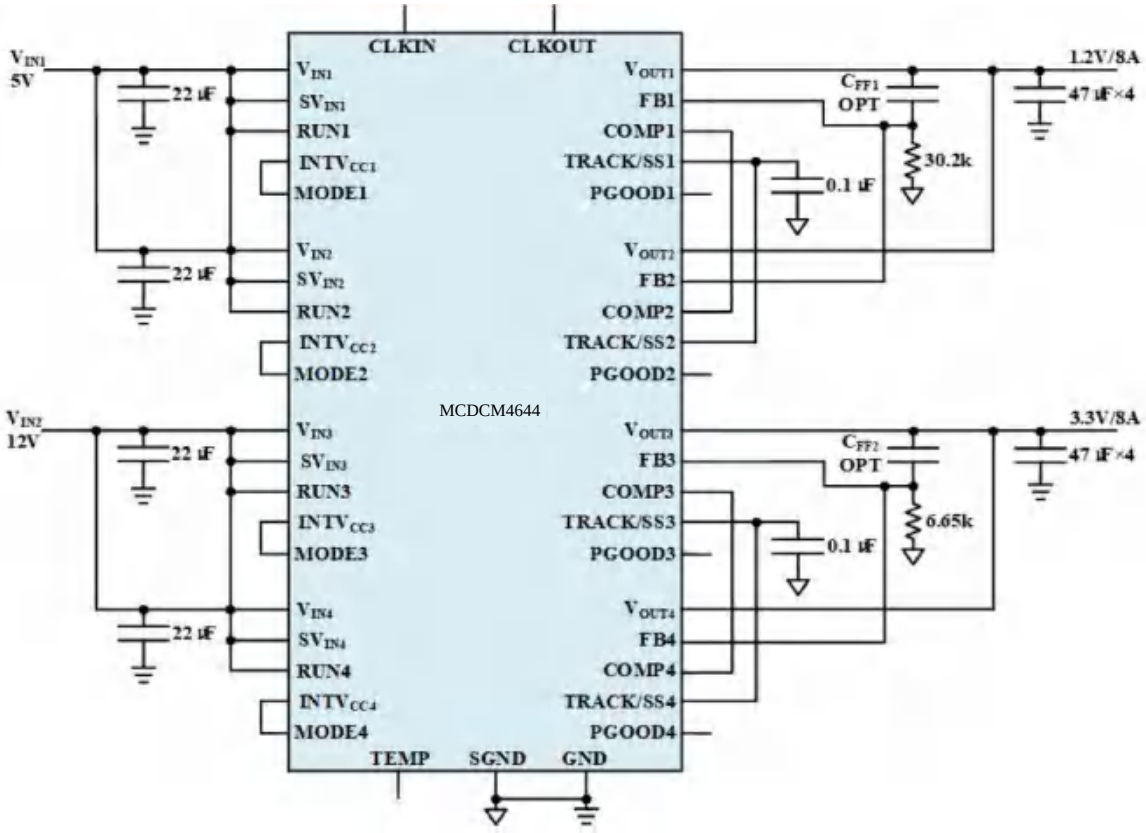


Figure 35. 2+2 Parallel Configuration, Load 8A

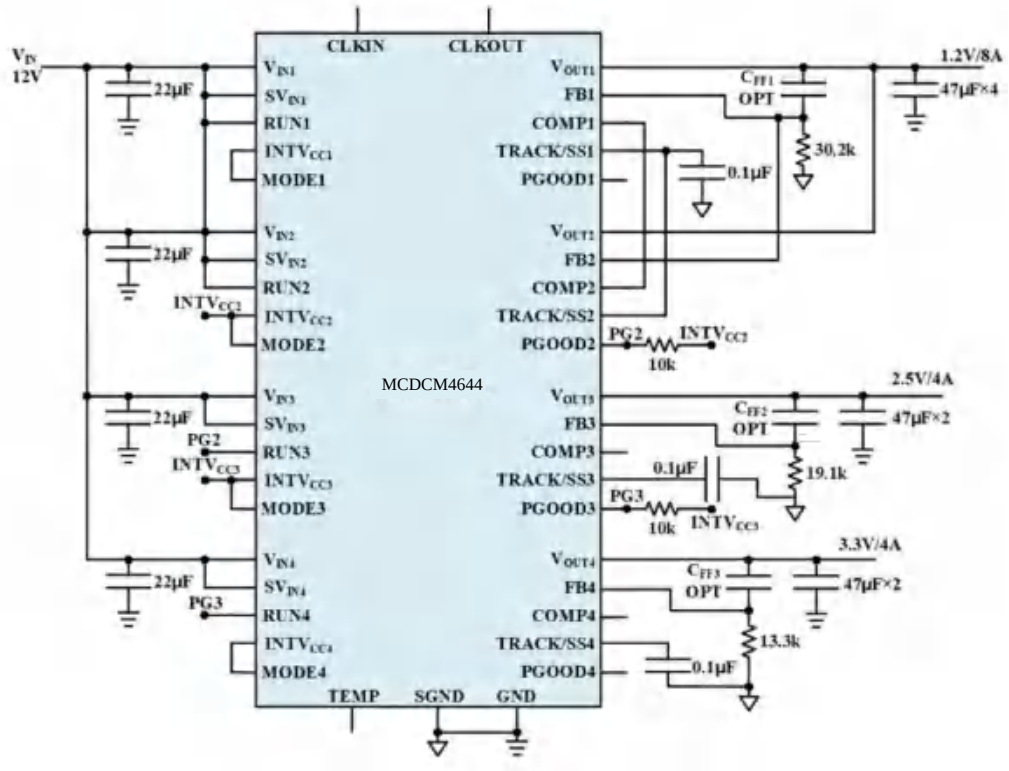


Figure 36. 2+1+1 Mode, PGOOD Controls Power-Up Sequence

Note 5: The typical application circuit (including the one on Page 1) is configured to maximize the module's optimal performance and is applicable to most scenarios. In practical applications, adjustments can be made based on board space constraints or output noise requirements. However, the input V_{IN}-to-ground capacitance per channel is not recommended to be lower than 10 µF, and the output capacitance should not be less than 47 µF, as values below these thresholds may degrade module stability. In addition to bulk capacitors, multiple smaller capacitors (e.g., 1 µF, 0.1 µF) can be added to filter high-frequency noise.

To suppress inrush current during startup, the TRACK/SS pin of each channel should not be left floating. A capacitor in the range of 10nF to 220nF is recommended for configuration on this pin.

The pull-up resistor for the PGOOD signal should be selected within the range of 4.7kΩ to 100kΩ. The capacitor between V_{OUT} and FB is a feed forward capacitor.

The MCDCM4644 is designed to ensure system loop stability without this capacitor. Adding a feedforward capacitor (typically 10pF to 100pF, with 47pF as a standard value) can improve phase margin and enhance stability. It is recommended to reserve space for this capacitor to allow flexibility during system debugging.

The 4A output current specified in the typical application circuit indicates the capability under limited test conditions. In actual use, derating must be applied according to the derating curves provided in the datasheet.

Product Size

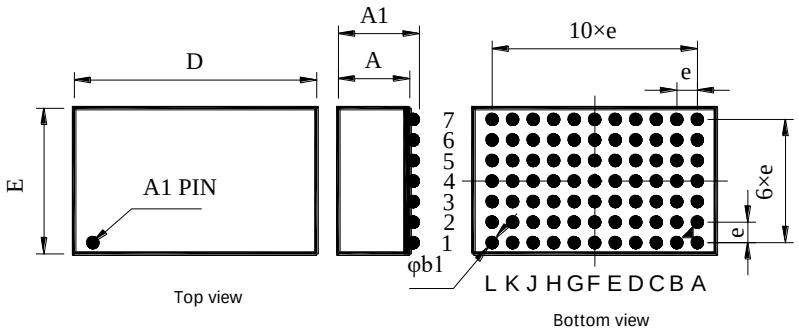


Figure 37. Dimensions of the Shape Unit: mm

Dimension Symbol	Value		
	Min	Nominal	Max
A	4.31	4.41	4.51
A1	4.80	5.00	5.10
D	14.8	15.00	15.20
E	8.80	9.00	9.20
Φb	0.53	0.63	0.73
Φb1	0.66	0.76	0.86
e	—	1.27	—

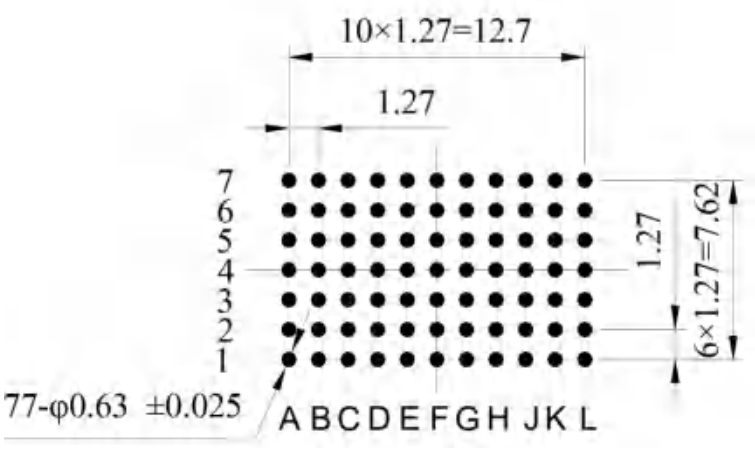


Figure 38. Recommended Pad Size Chart for PCB

Electronics Assembly Instructions

Storage Requirements

For long-term storage, seal the product in an anti-static bag with desiccant under vacuum and store it in an electronic dry cabinet.

If stored post-unsealing under conditions of 30°C and 60% relative humidity (RH), the maximum allowable duration is 168 hours. Products exceeding this period must be baked according to the procedures outlined in IPC/JEDECJ-STD-033 before use or storage. After baking, it is recommended to complete assembly processes (e.g., reflow soldering) within 48 hours. For devices without specified requirements, store in a nitrogen dry cabinet.

Recommended Environmental Process Conditions

1. Product Pre-Treatment

For plastic-encapsulated modules: pre-bake at 125° C for 48 hours before use, or follow IPC/JEDECJ-STD-033B *"Handling, Packaging, Shipping, and Use of Moisture/Reflow-Sensitive Components"* to ensure moisture removal. Complete reflow soldering within 48 hours after baking.

2. Soldering Materials

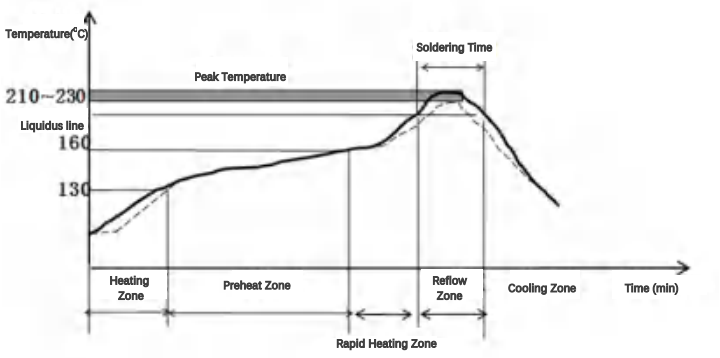
For lead-based soldering, it is recommended to use lead-based solder paste compositions such as Sn63Pb37 or Sn62Pb36Ag2. For lead-free soldering , the use of lead-free solder paste, specifically Sn96. 5Ag3Cu0.5, is advised. The solder paste should comply with a grade of 3 or higher.

3. Component Placement

Align the module's pad centers precisely with the corresponding PCB pads. The solder balls/pads should be pressed into the solder paste to a depth of approximately 0.05mm. Adjust placement pressure to ensure proper contact between pads and solder paste without squeezing paste beyond the pad boundaries. Solder voiding must not exceed 25%.

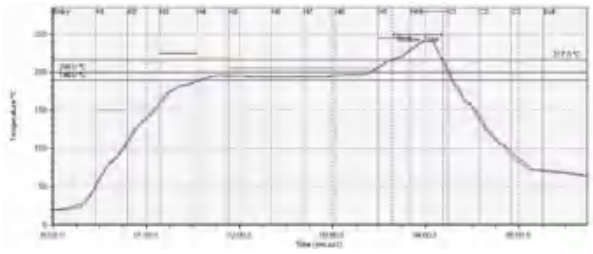
4. Recommended Reflow Profiles

The module is compatible with both lead-based (see Figure 39) and lead-free (see Figure 40) reflow profiles . Use a 9-zone or higher reflow oven to ensure uniform temperature distribution(Note6)



No.	Item	Condition
1	Maximum temperature rise slope in preheat zone	≤3°C/s
2	Maximum temperature drop slope in preheat zone	≤4°C/s
3	Preheat zone duration (130~160°C)	60s~120s
4	Peak temperature in reflow zone	210°C~230°C
5	Reflow zone duration (time ≥183°C for Sn63Pb37)	30s~90s

Figure 39. Typical lead-based reflow soldering profile and parameters.



No.	Item	Condition
1	Heating rate	≤3°C/s
2	Soak zone temperature range	≤4°C/s
3	Soak time	60s~120s
4	Peak temperature	240°C~245°C
5	Time above liquidus (>217°C)	30s~90s
6	Cooling rate	<5°C/s

Figure 40 Typical lead-free reflow soldering profile and parameters.

Note 6: During soldering, the parameters above may be optimized based on the actual component layout. However, the peak temperature must not exceed 245°C. If thick or large metal components require temperatures exceeding 245 °C, thermal shielding measures must be applied to the power module to ensure the actual soldering temperature does not exceed 245°C.

5. Cleaning Clean

using a water-based cleaning agent, followed by drying. Users may adjust the soldering and cleaning processes based on actual conditions, but ultrasonic cleaning is not recommended.

6. Inspection

Inspect the appearance under a microscope to ensure compliance with requirements.

7. X-ray Imaging

Perform X-ray inspection to check solder joint positions, verify solder void compliance, and detect any short circuits. After confirming compliance of the first 1-3 samples, proceed with batch reflow soldering.

Trouble shooting

If a suspected malfunction is observed after device assembly, perform the following checks:
Open Circuit: Inspect solder joints for cold solder joints, insufficient pin soldering, or poor soldering.
No Output: Check the output capacitors near the module.
Short Circuit: Use X-RAY to inspect for internal or external short circuits.

Removal Process

Before removing the product module from the PCB , bake the PCB at 125°C for 48 hours to ensure the module remains unaffected. If baking is omitted, there is a risk of delamination between the plastic module and the substrate. In severe cases, internal solder may melt and flow through delamination gaps, leading to module failure.
For module removal, use a BGA rework station. Handheld hot air guns are not recommended (temperature may exceed 245°C). The product may only be reworked once.

Precautions

The device must be handled with anti-static measures. Wear anti-static gloves when handling the module to prevent electrostatic discharge (ESD) damage caused by human body charges.
Recommended Operational Practices:
a) Operate the device on an anti-static workbench or use finger cots.
b) Ensure all testing equipment and tools are properly grounded.
c) Avoid touching the device leads directly.d) Store the device in anti-static containers (e.g., ESD-safe boxes).
e) During production, testing, usage, and transportation, avoid materials that generate static electricity (e.g., plastics, rubber, silk fabrics).
f) Maintain relative humidity between 30%~70%.